SIFA on Nonce-based Authenticated Encryption: When does it fail? Application to Ascon

Viet-Sang Nguyen

joint work with Vincent Grosso and Pierre-Louis Cayrel

SESAM Seminars
Saint-Étienne, 3 July 2025

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Laboratoire Hubert Curien
UMR ▪ CNRS ▪ 5516 ▪ Saint-Étienne

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PROPHY ANR-22-CE39-0008-01

What is SIFA?

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Statistical Ineffective Fault Attack

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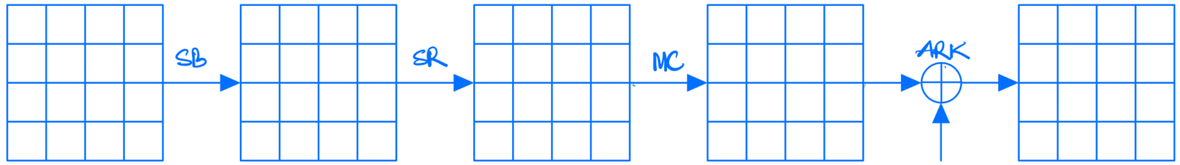
Statistical Ineffective Fault Attack

But what is it exactly? 🤔

Example on AES

- State: 4x4 bytes



- Operations in a round:
  - SB: SubBytes
  - SR: ShiftRows
  - MC: MixColumns
  - ARK: AddRoundKey

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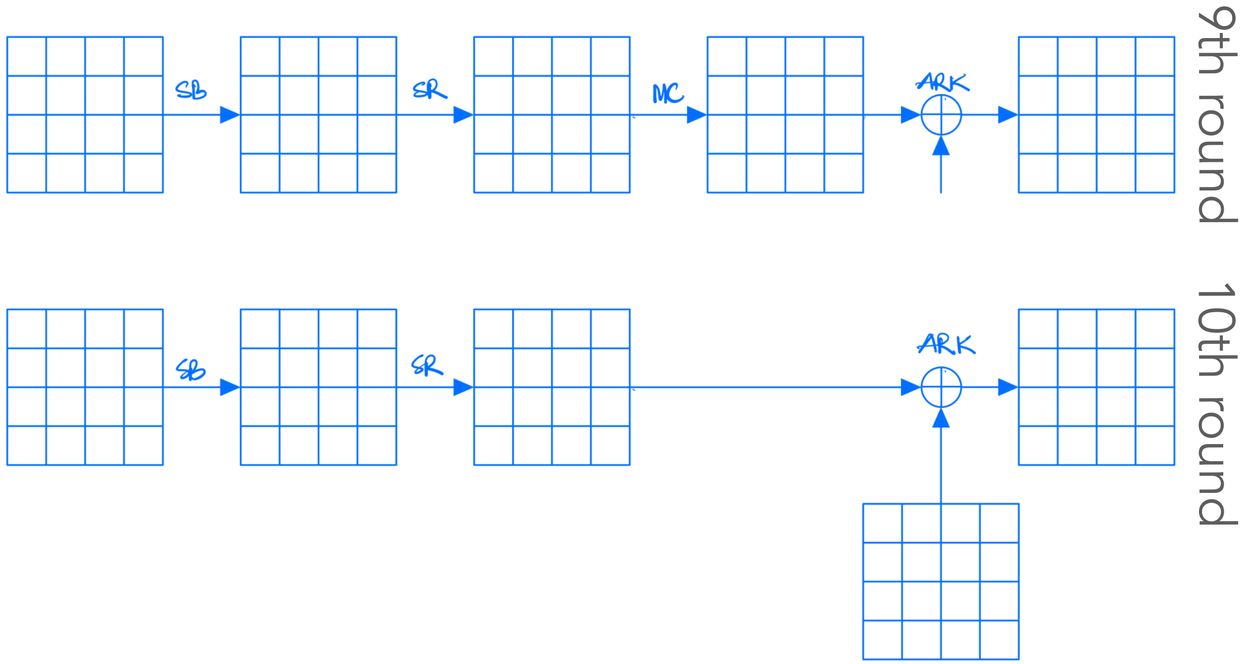

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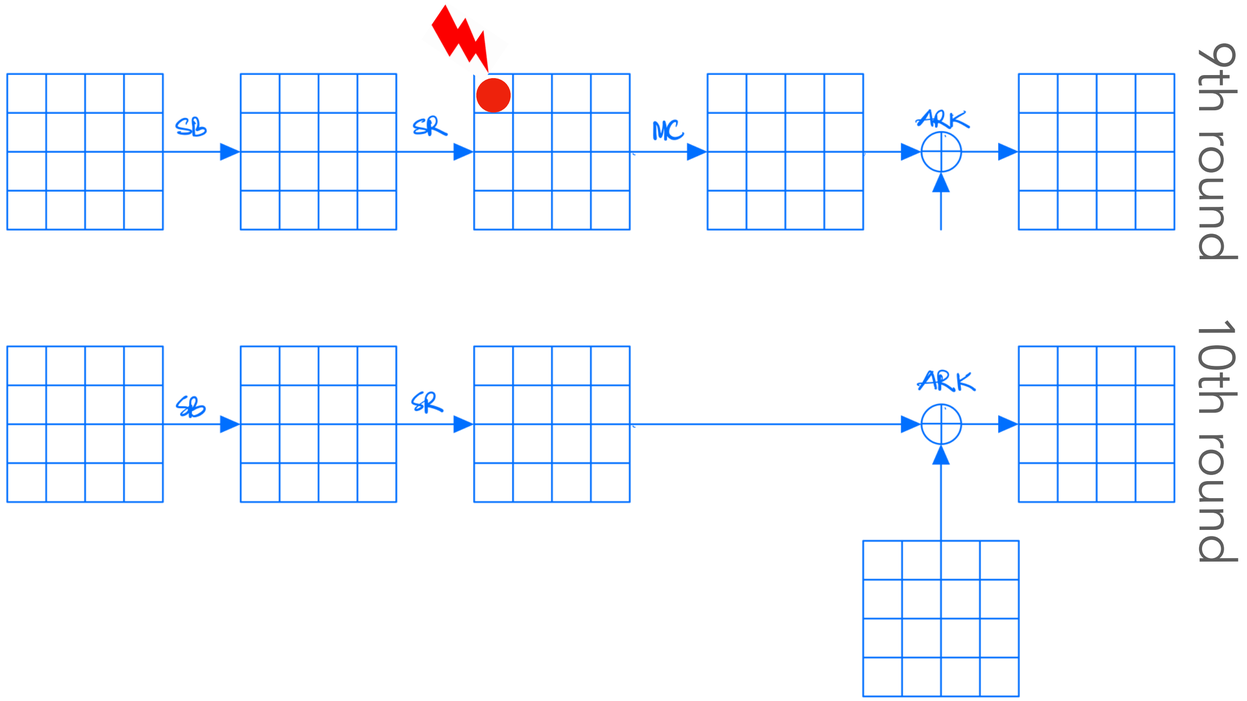

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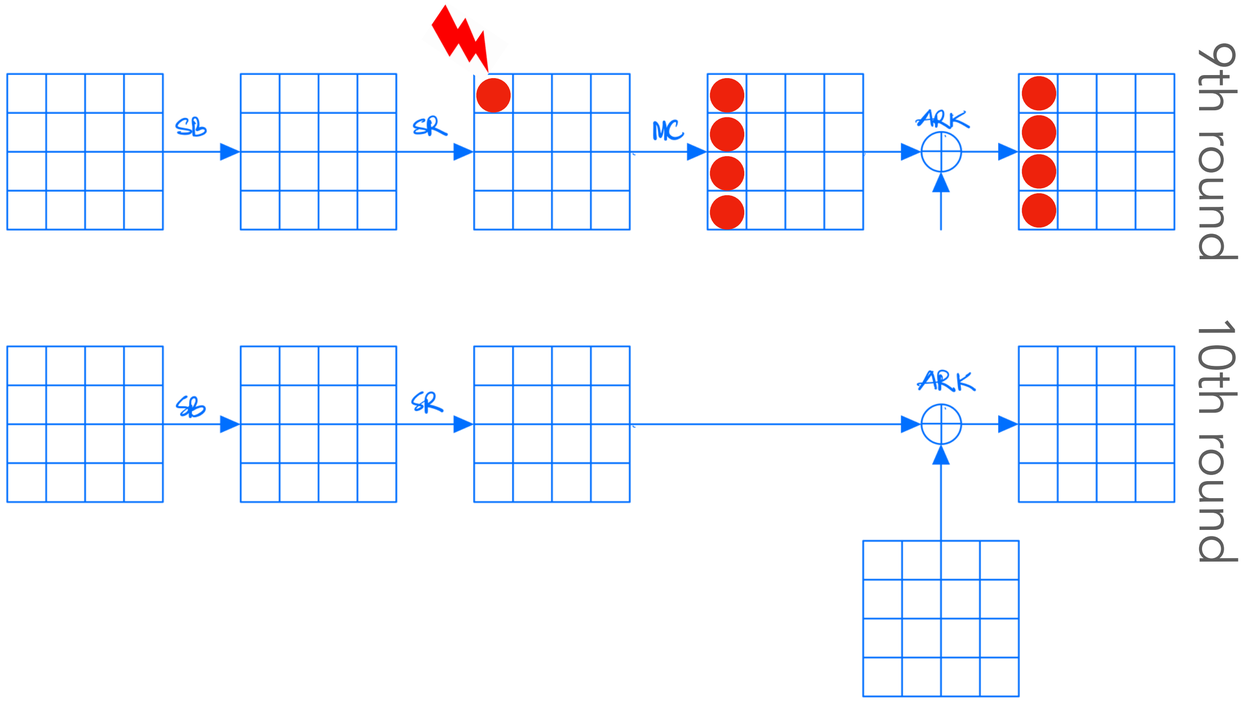

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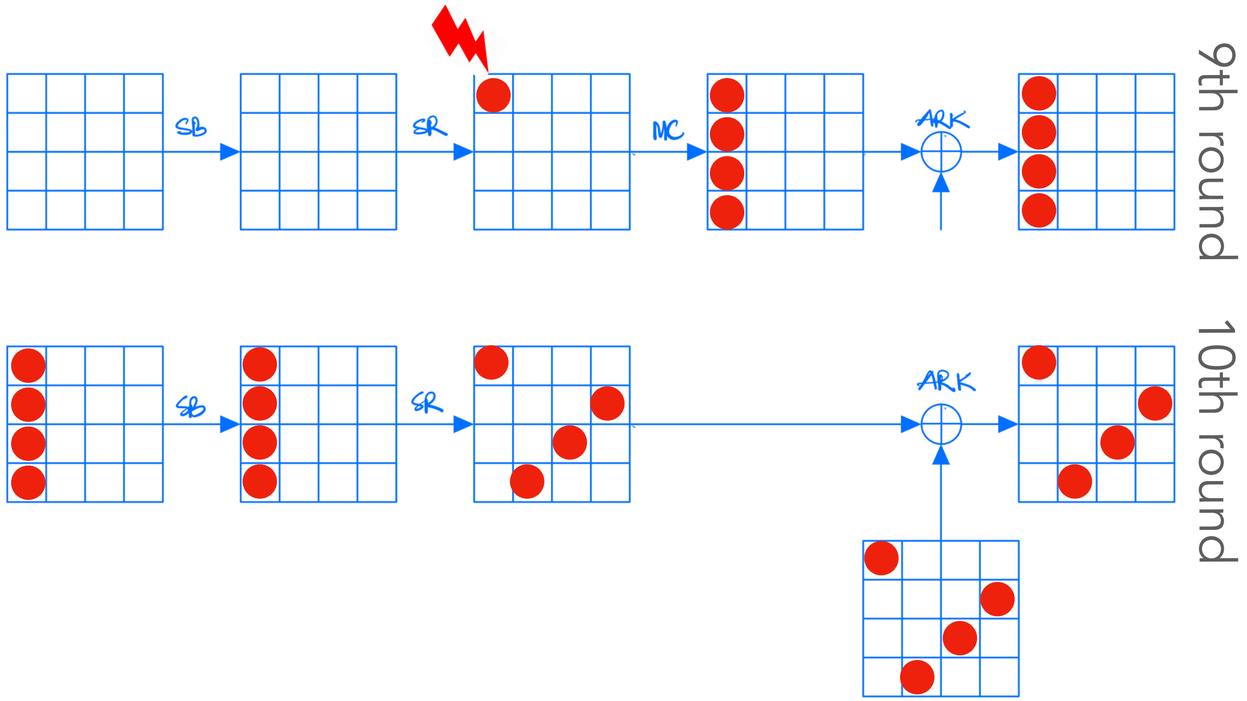
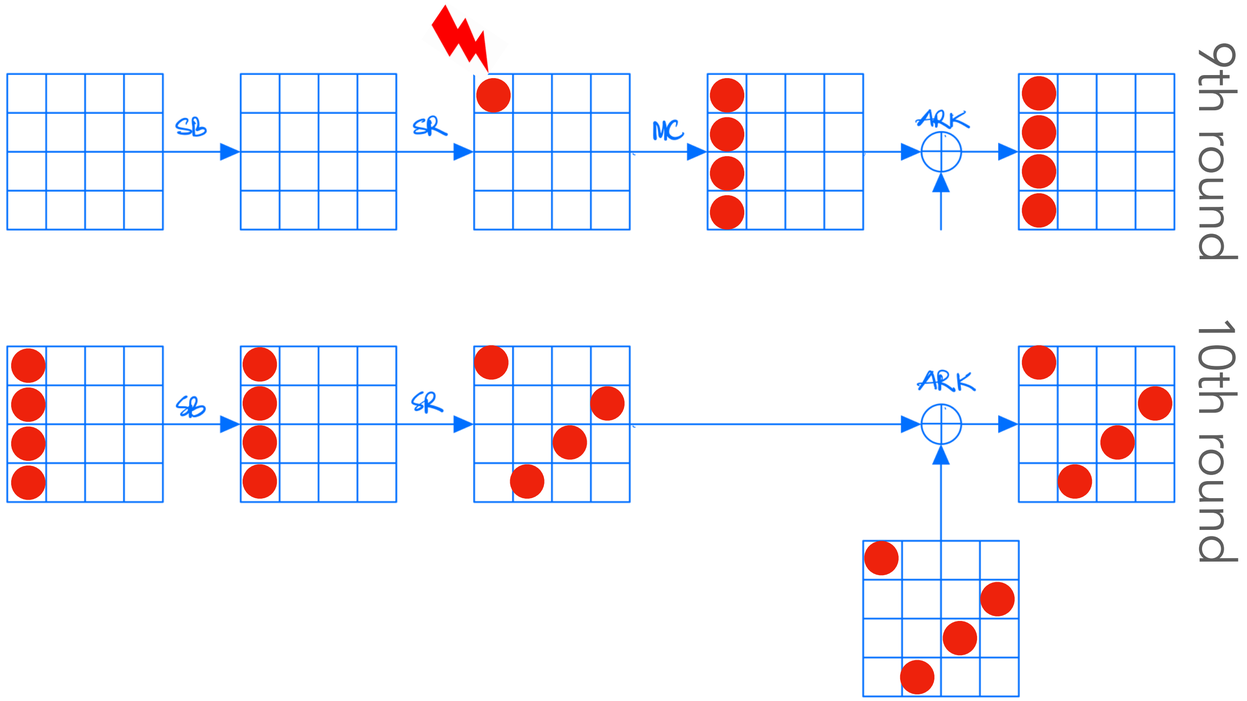


Example on AES

- Choose an intermediate value v
- Cause v biased by faults (e.g., stuck-at-0)
- Collect a number of ciphertexts



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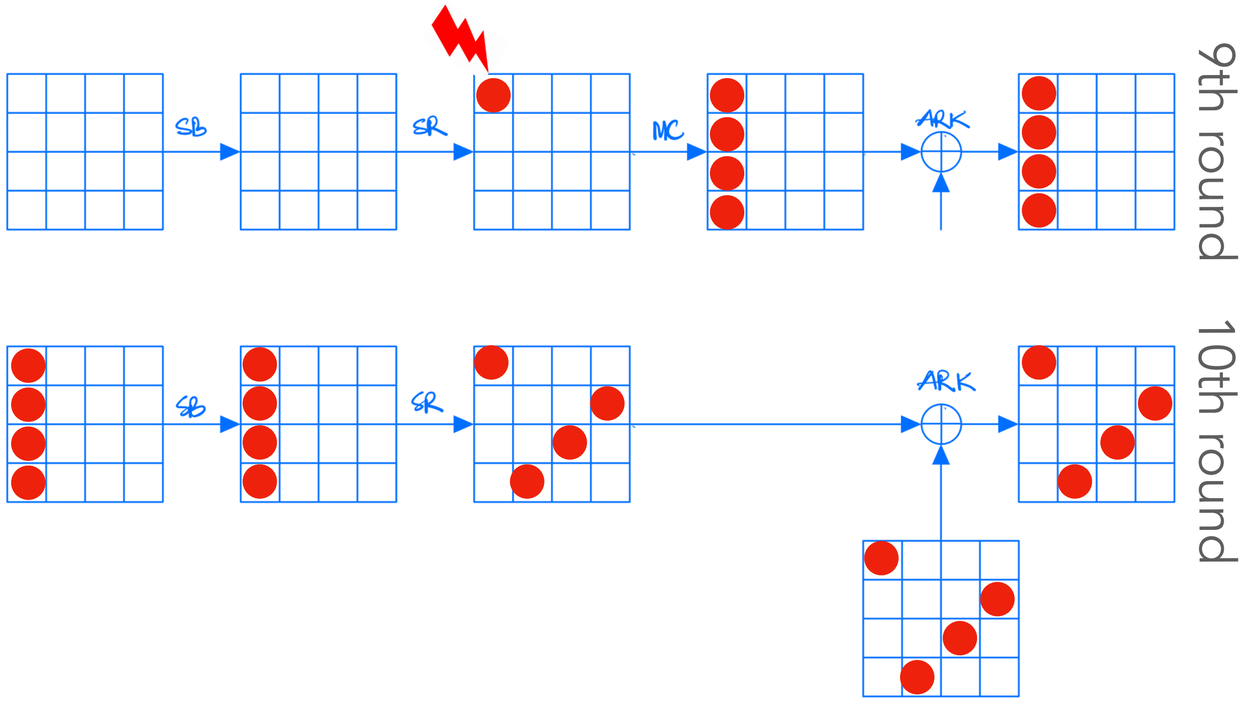

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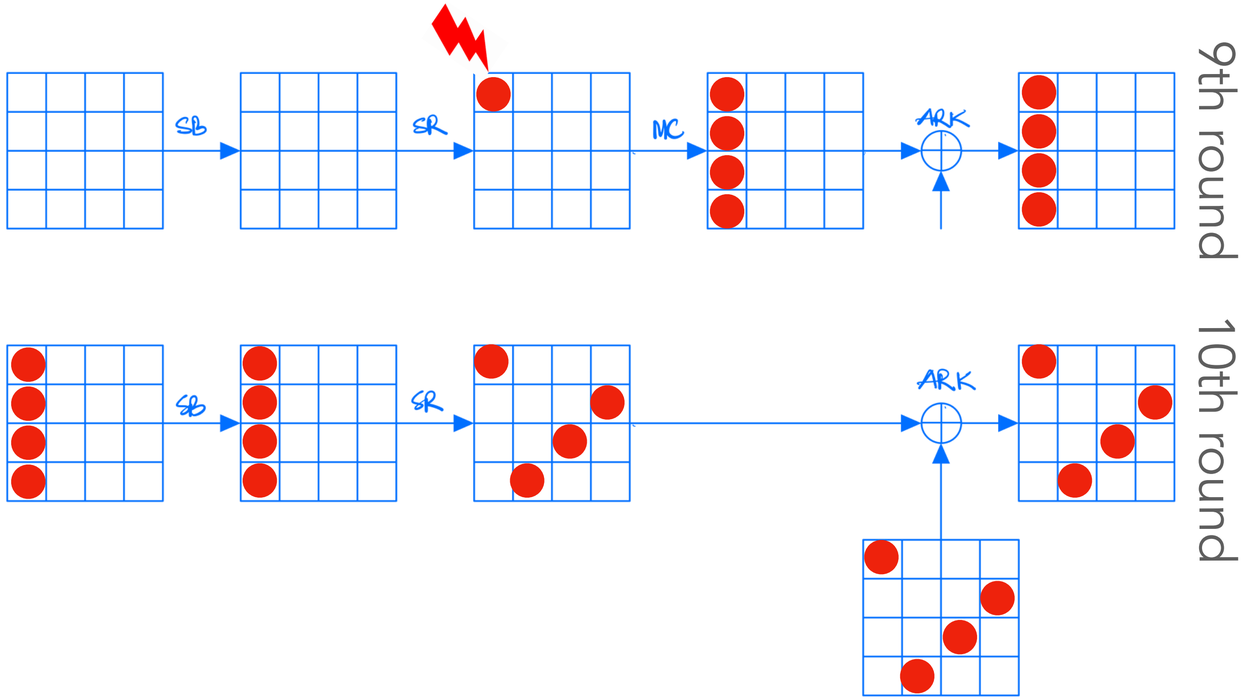

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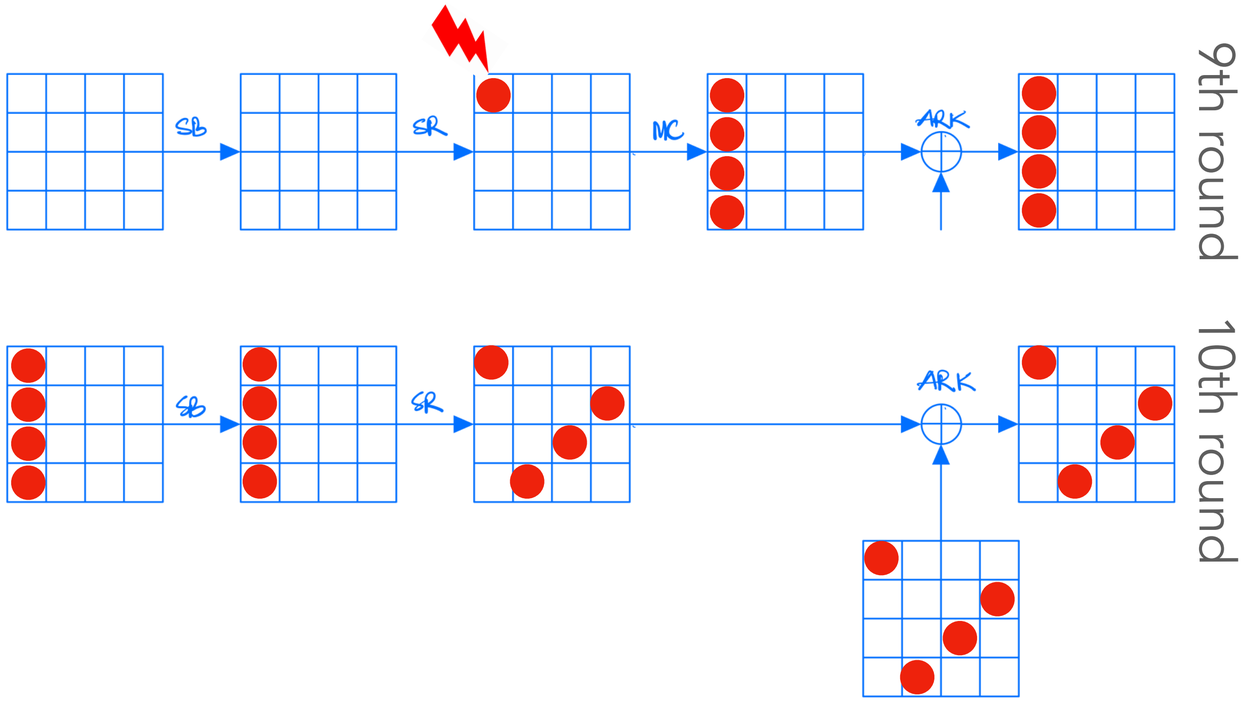

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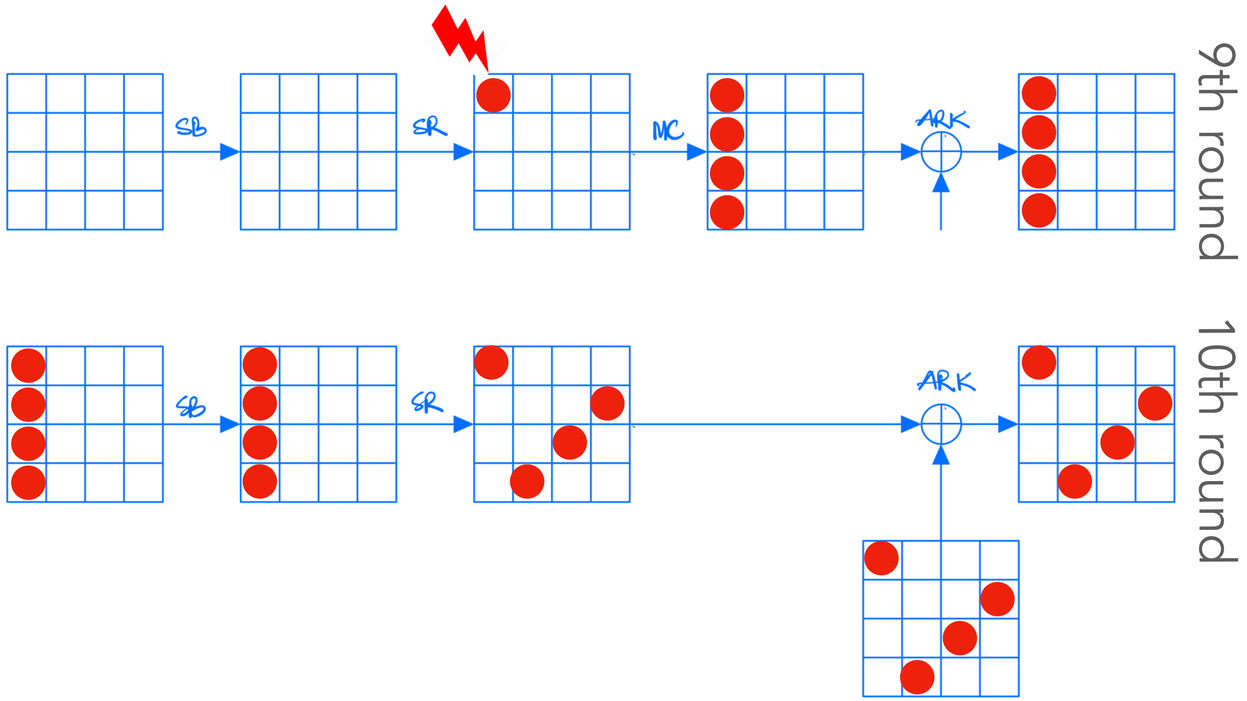

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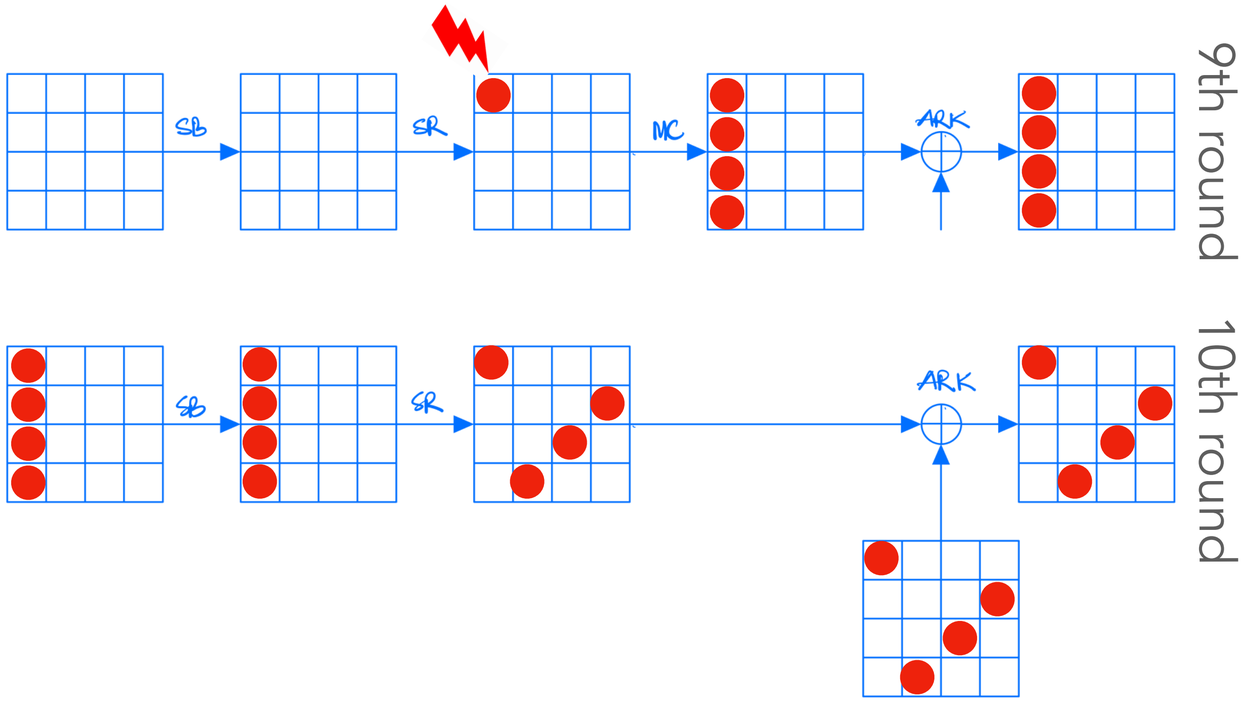

Statistical Fault Attack (SFA) by Fuhr et al., 2013

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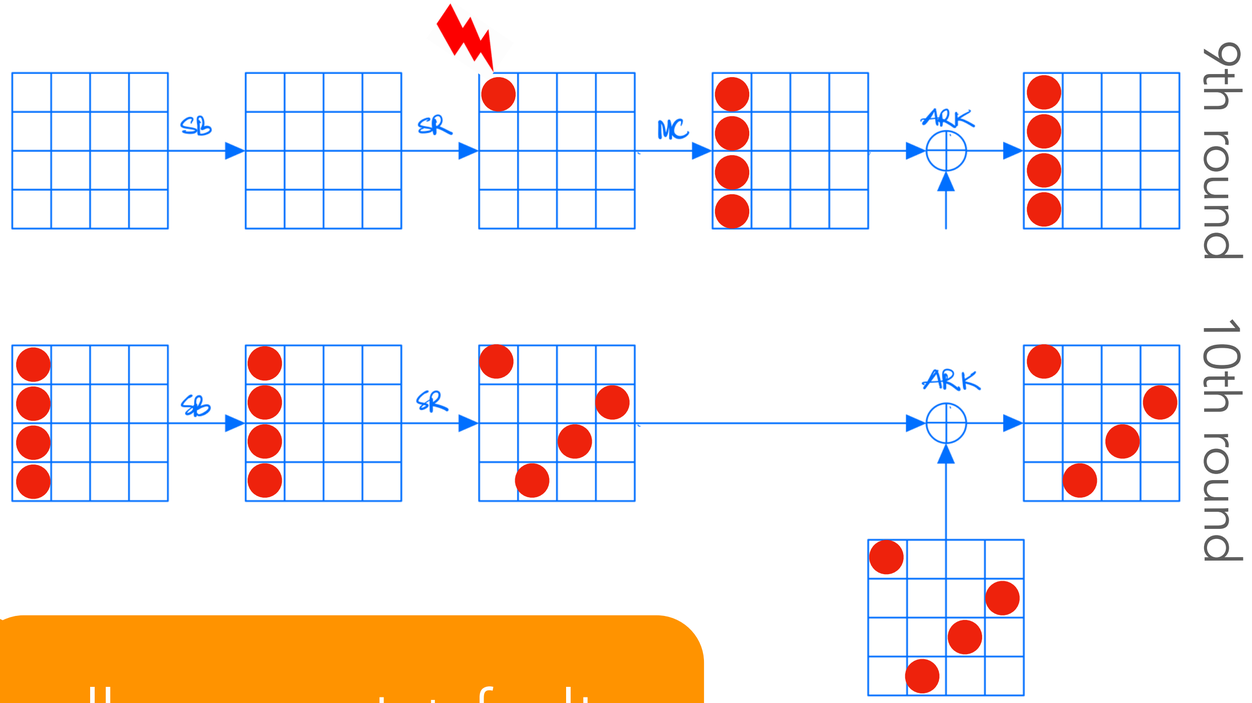

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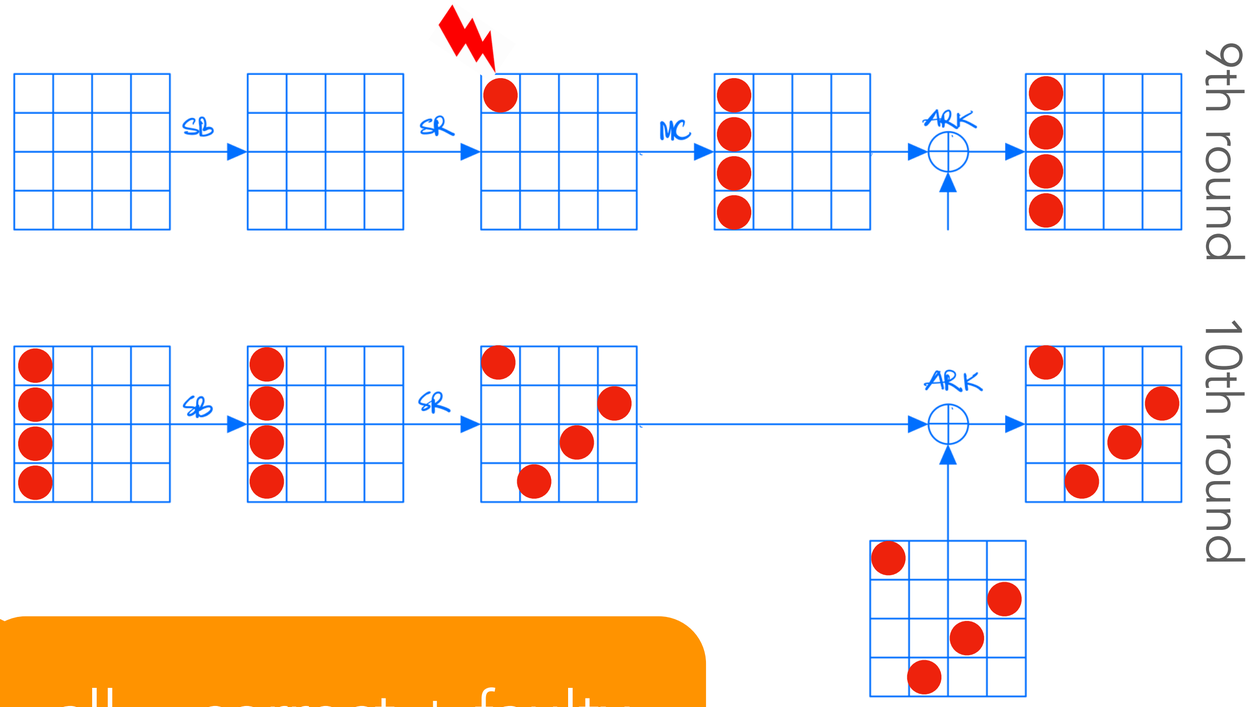

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When a countermeasure is used...

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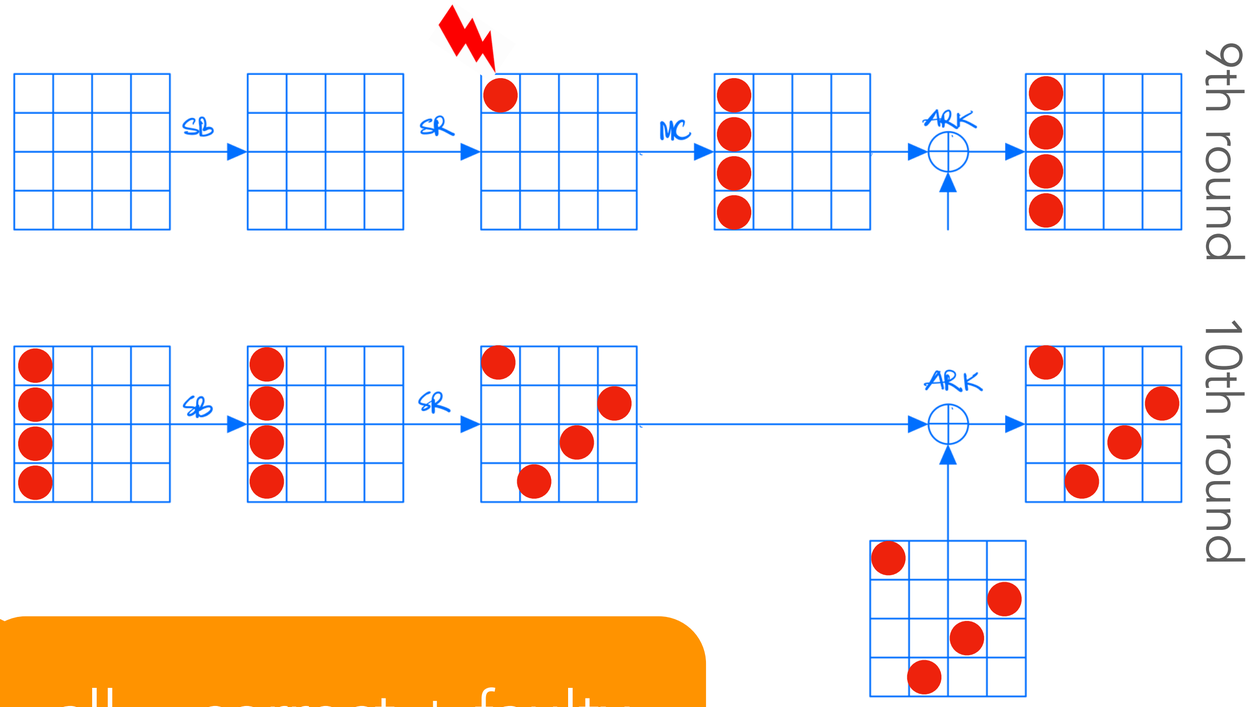

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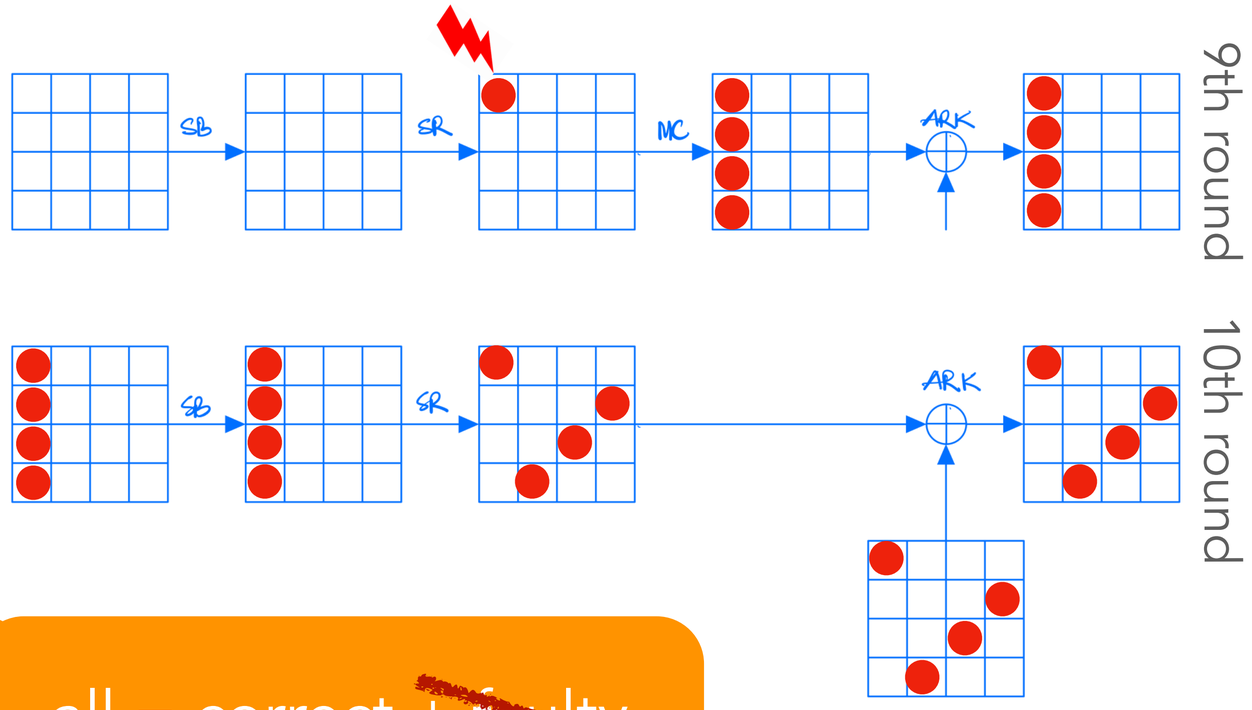

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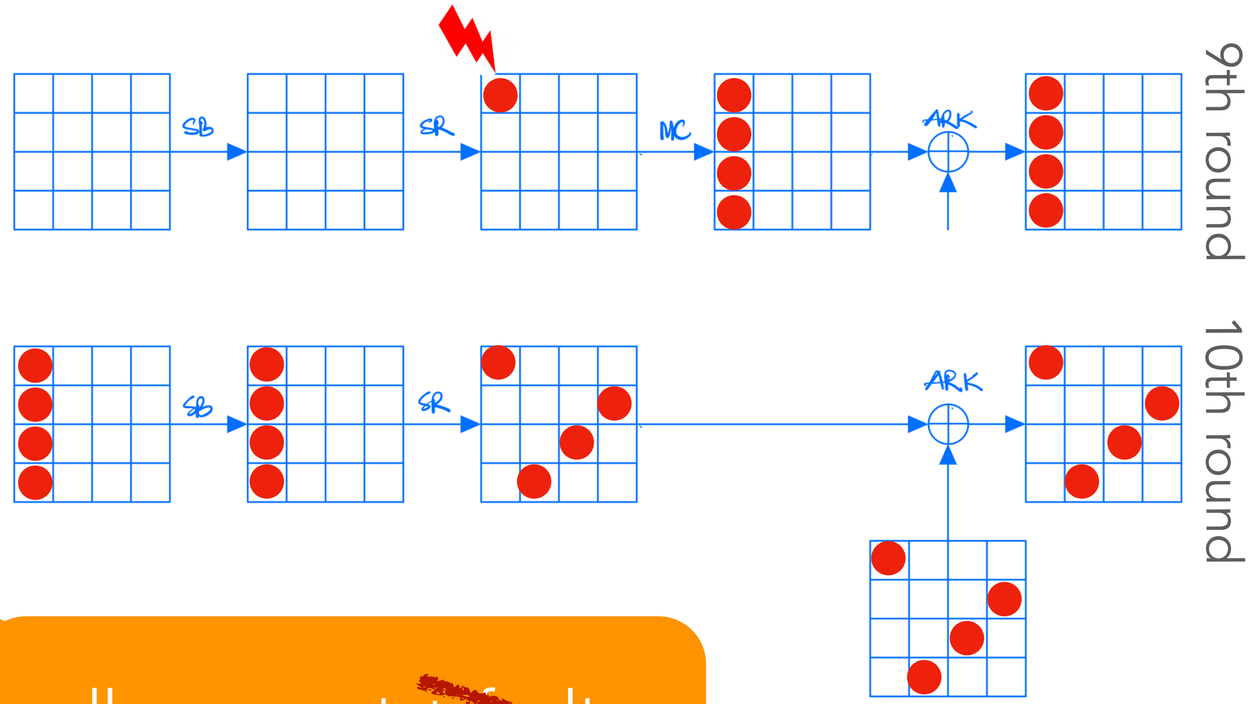

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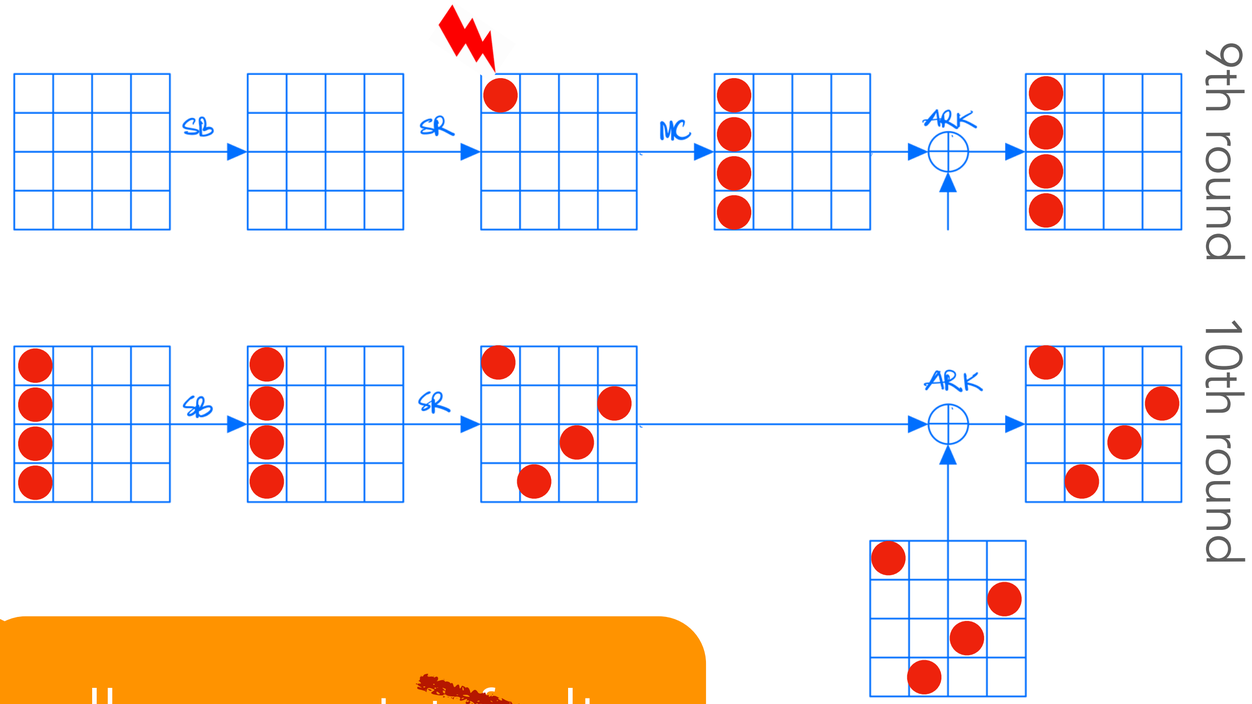

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biased distribution of ineffective faults

SIFA on Nonce-based Authenticated Encryption

Dobraunig et al., 2019

Fault Attacks on Nonce-based Authenticated Encryption: Application to Keyak and Ketje

Christoph Dobraunig[1], Stefan Mangard[1], Florian Mendel[2], and Robert Primas[1]

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Hum, let's try ! 😈

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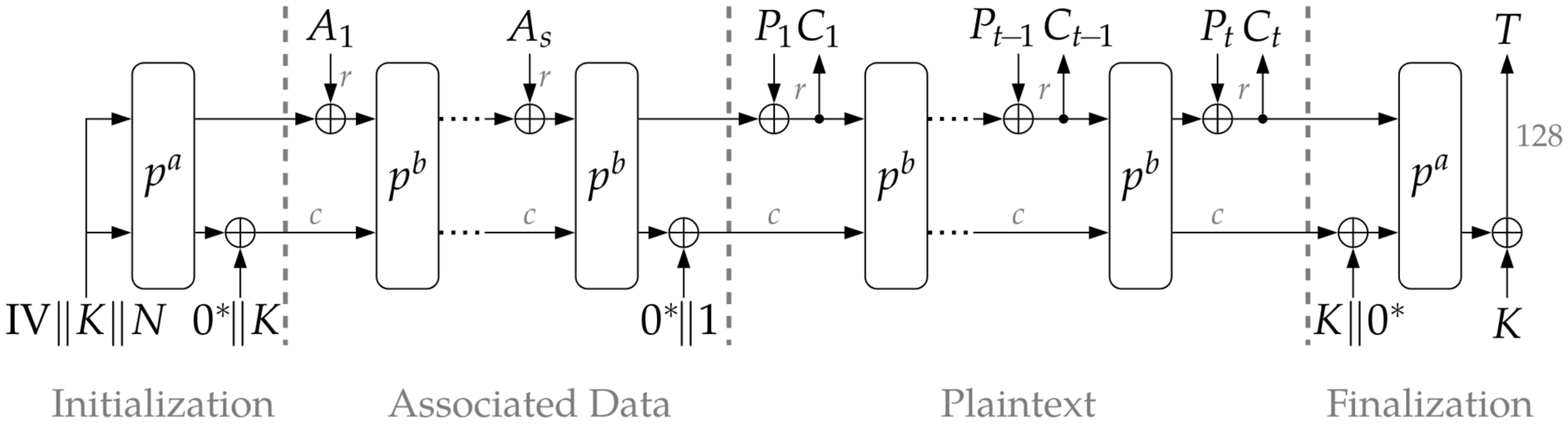
Ascon


A_1
A_s
$P_1 C_1$
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T
r
c
p^a
p^b
128
$\mathrm{IV} \| K \| N$
$0^* \| K$
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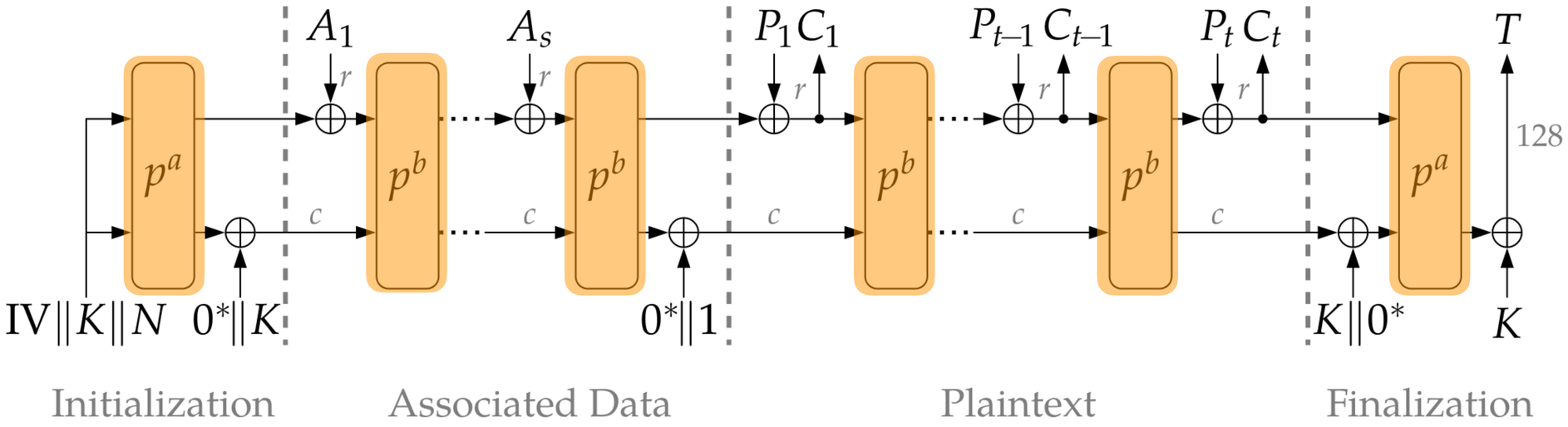
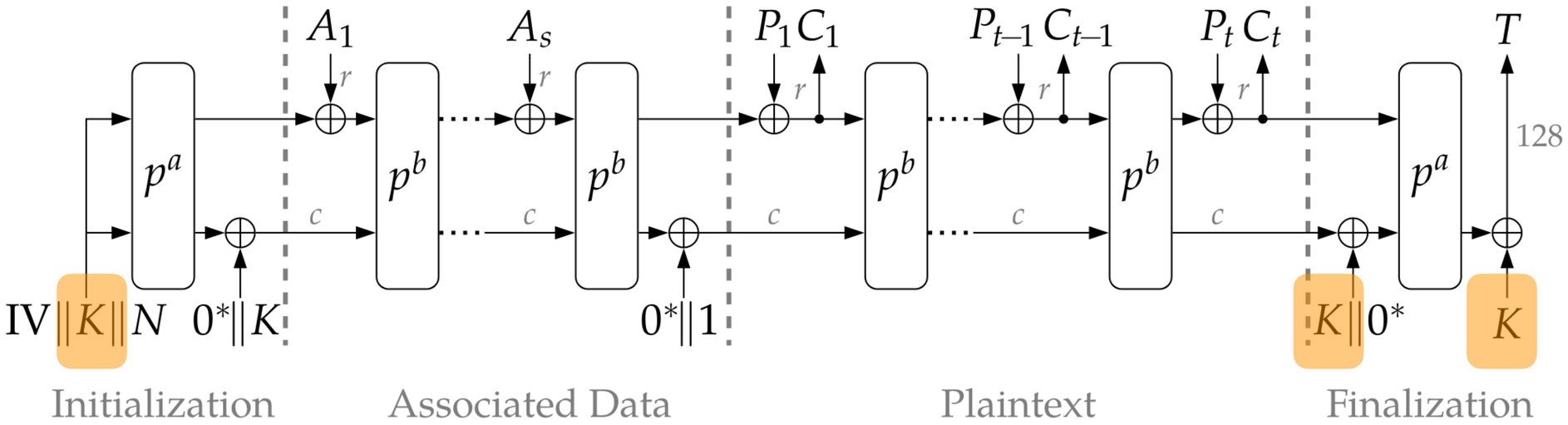
K
Initialization
Associated Data
Plaintext
Finalization

Permutation blocks



- p^a: 12 permutation rounds ($a = 12$)
- p^b: 8 permutation rounds ($b = 8$)

Key (128 bits)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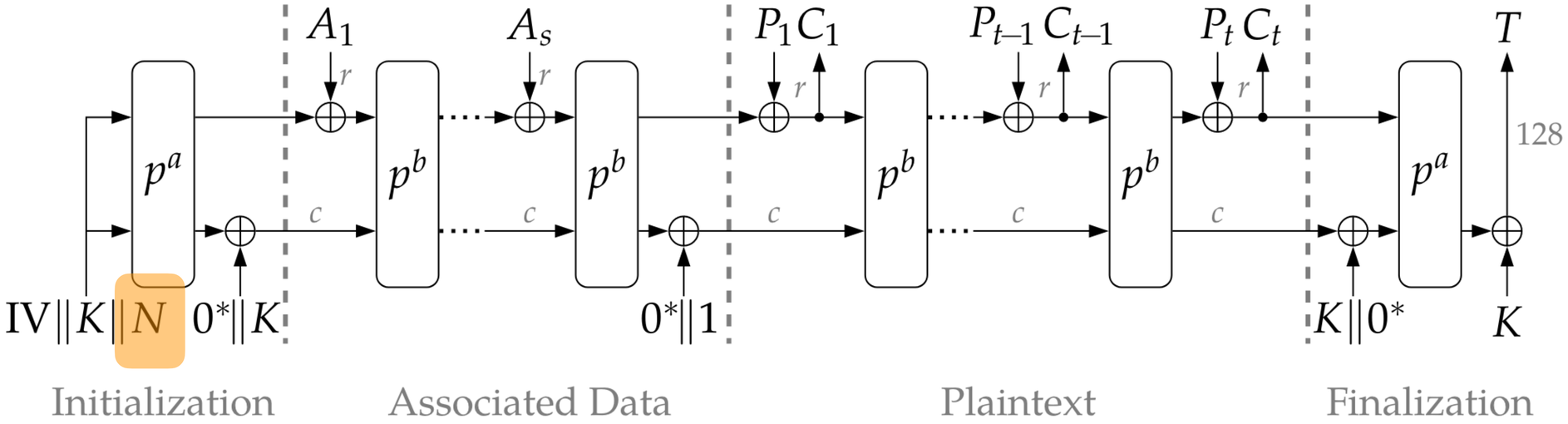
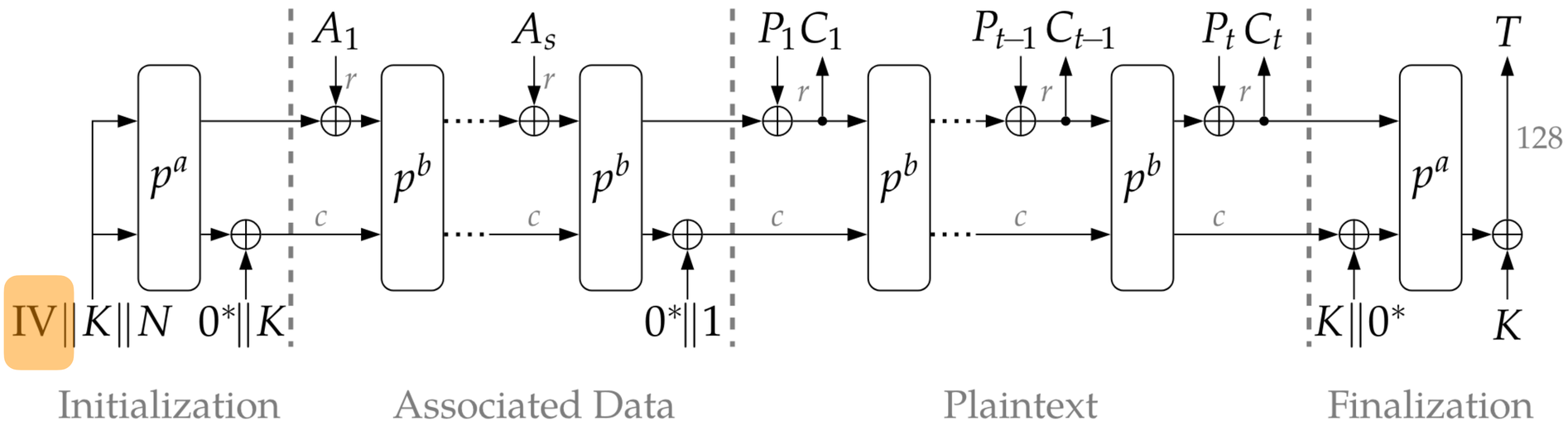
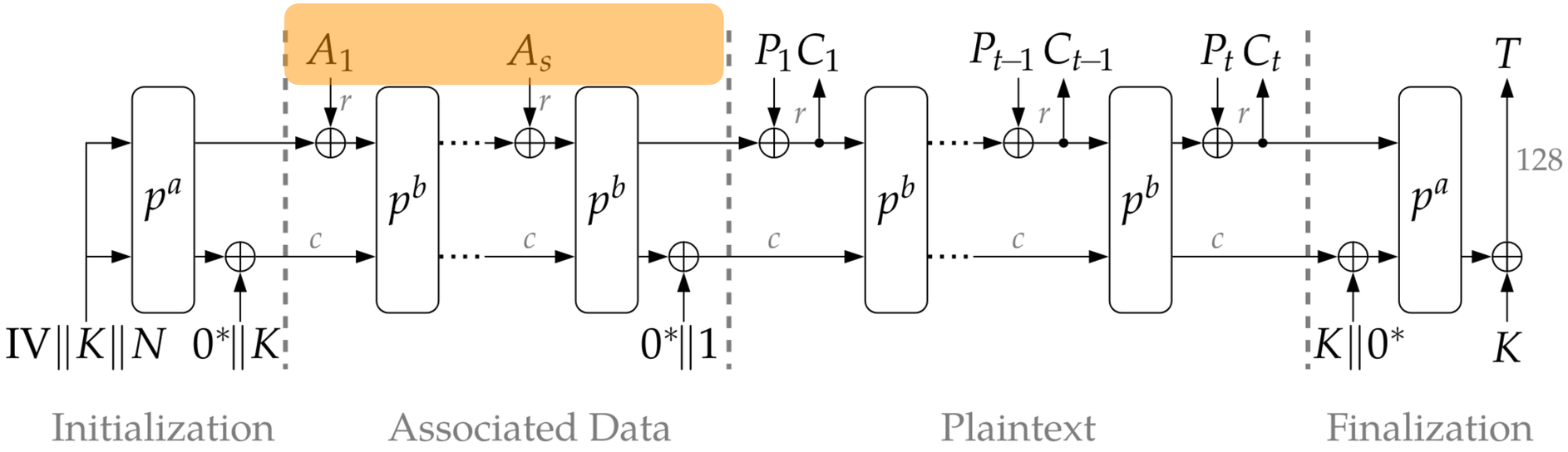
Nonce (128 bits)



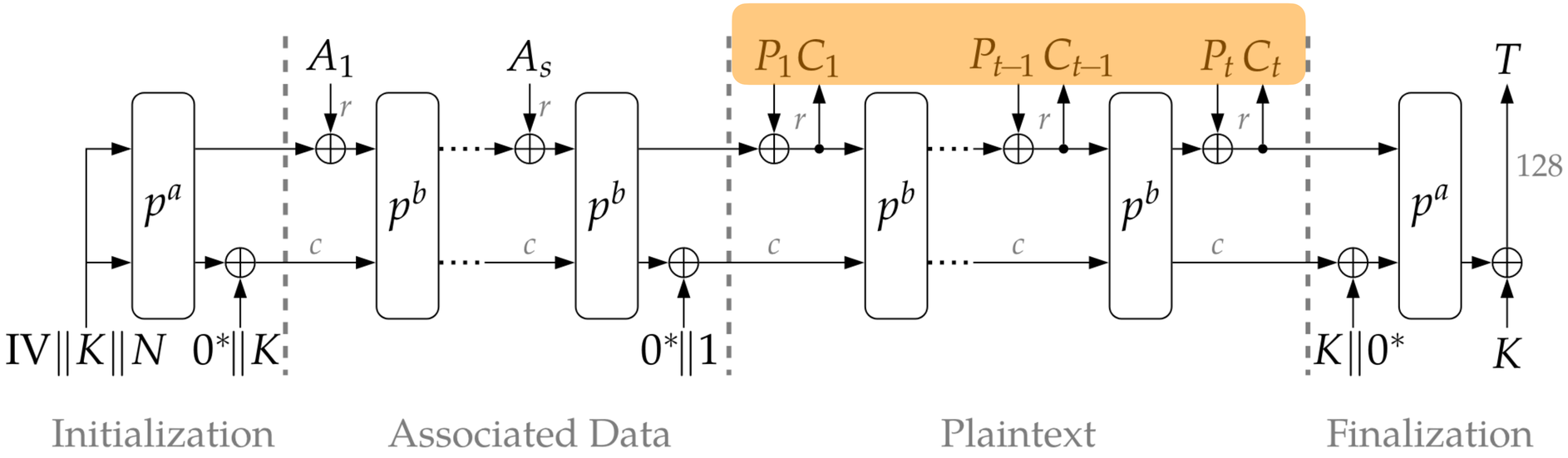
Initialization vector



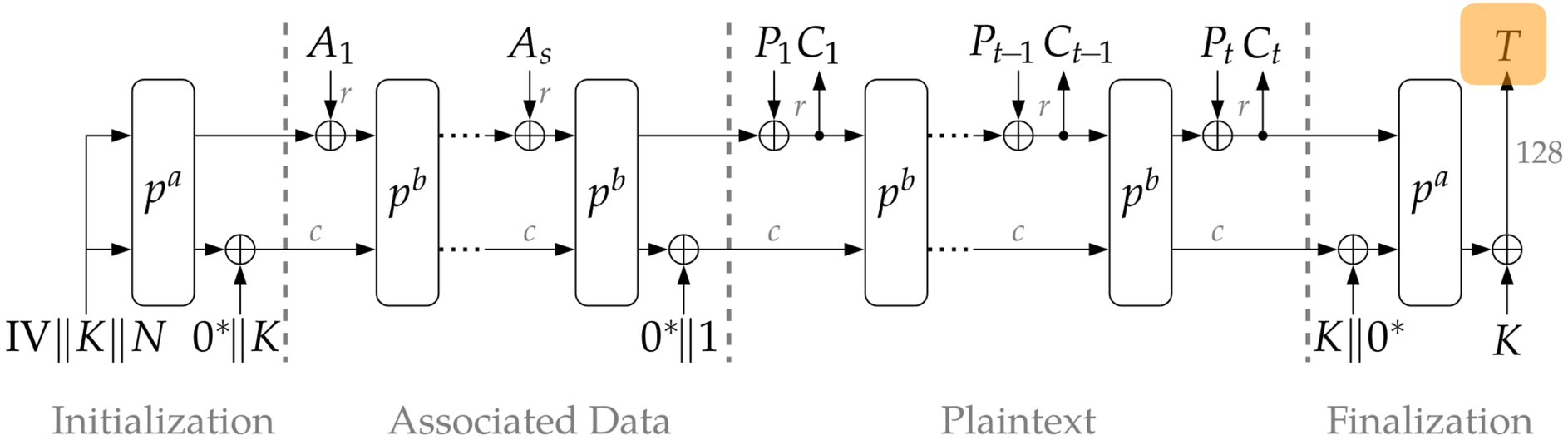
Associated data

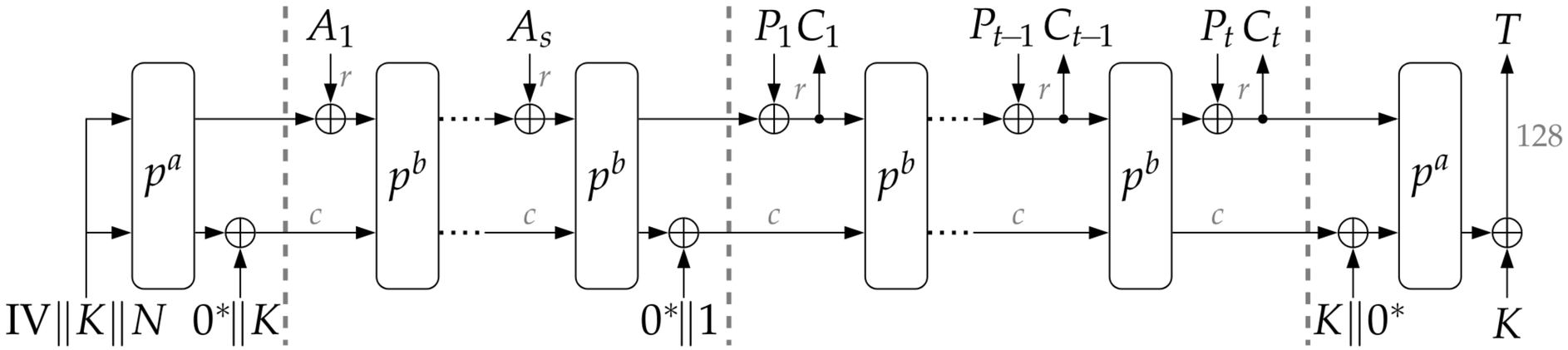


Plaintext / Ciphertext



Verification tag

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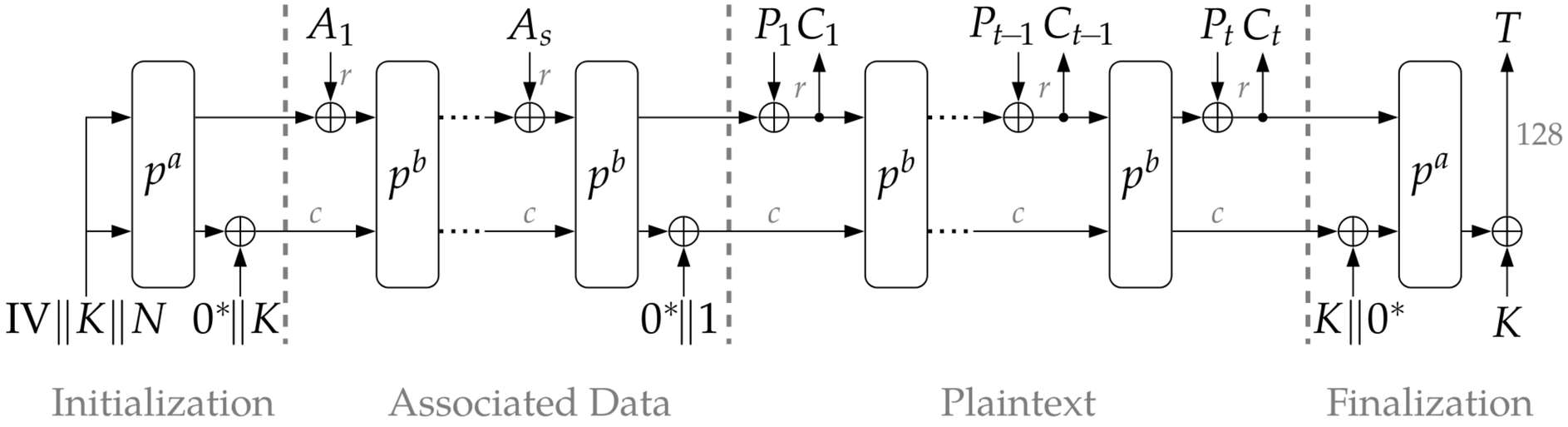
Focus on 1st round of initialization



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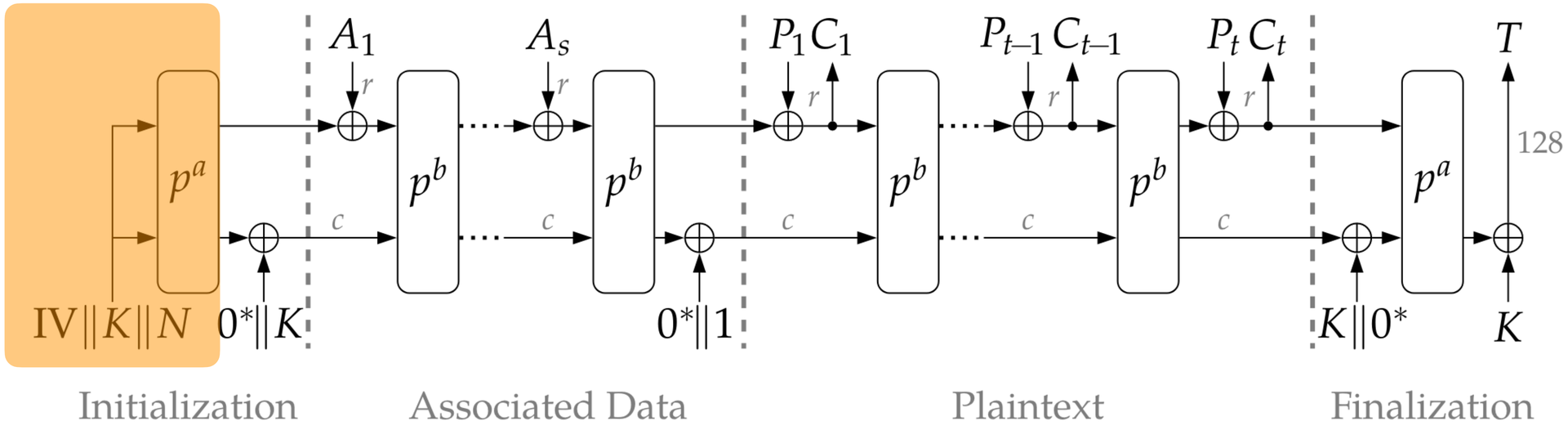

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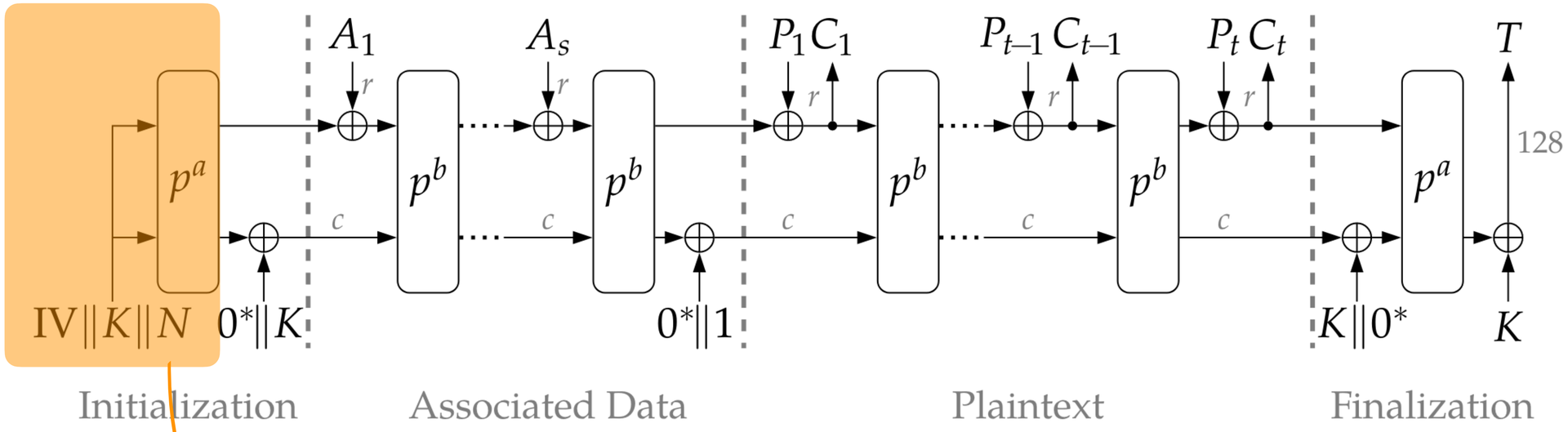

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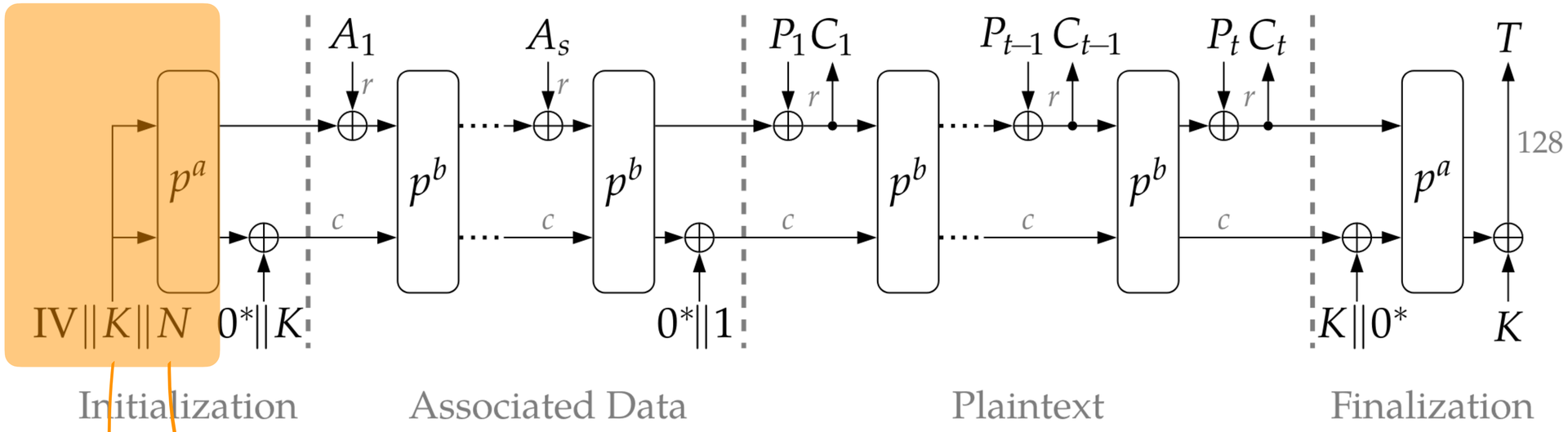
Focus on 1st round of initialization



Control the nonce N

Guess the key K

1st round computation

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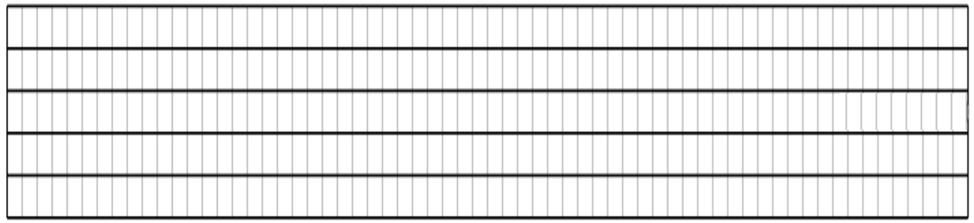
On 320-bit state = 5 x 64-bit words



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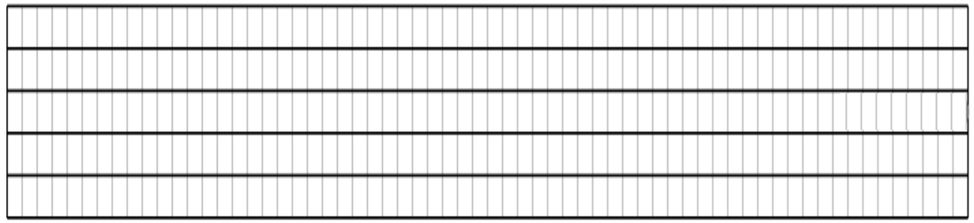
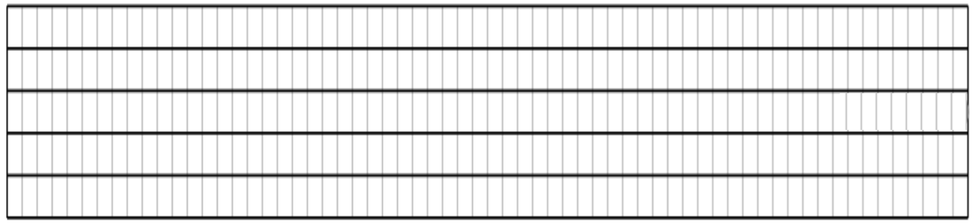


Input of the first round:

1st round computation

On 320-bit state = 5 x 64-bit words



Input of the first round:

- 128-bit key : $K = (k_0, k_1)$
- 128-bit nonce : $N = (n_0, n_1)$
- 64-bit init. vector : IV

1st round computation

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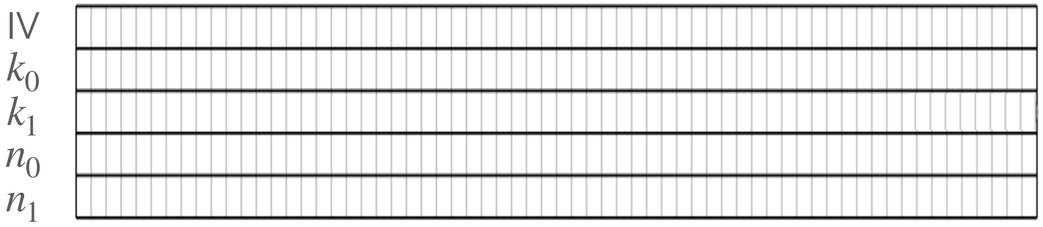

Input of the first round:

- 128-bit key : $K = (k_0, k_1)$
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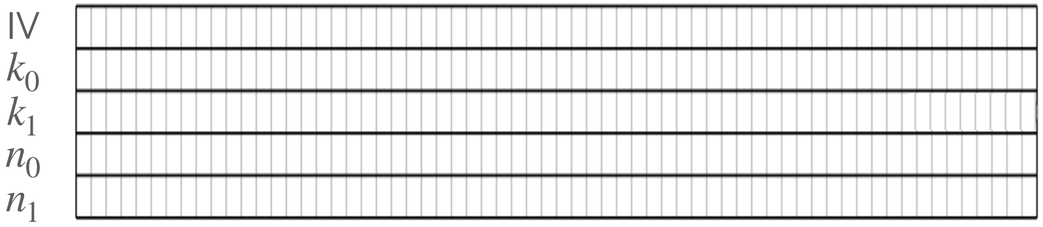
1st round computation

On 320-bit state = 5 x 64-bit words



Input of the first round:

- 128-bit key : $K = (k_0, k_1)$
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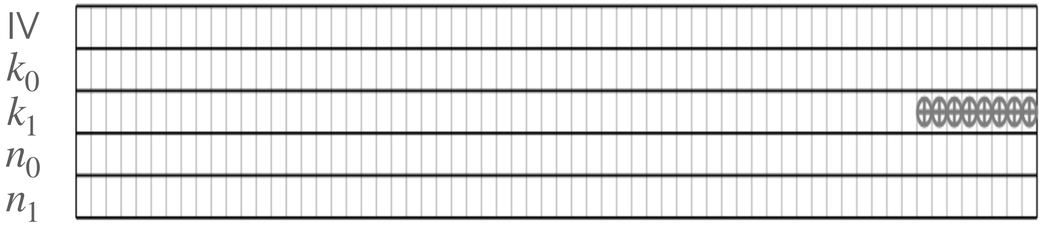
- 64-bit init. vector : IV

3 operations in a round

1st round computation

On 320-bit state = 5 x 64-bit words



(1) Constant addition

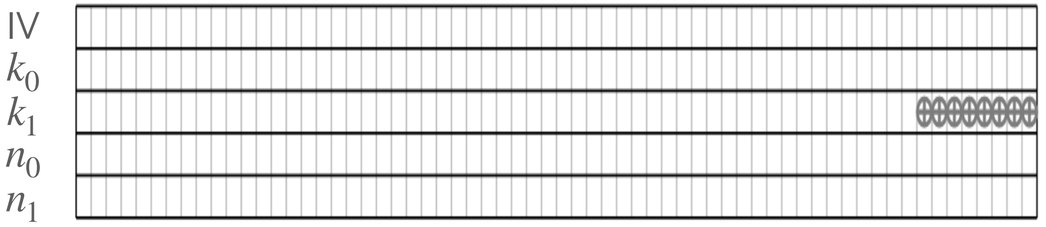
Input of the first round:

- 128-bit key : $K = (k_0, k_1)$
- 128-bit nonce : $N = (n_0, n_1)$
- 64-bit init. vector : IV

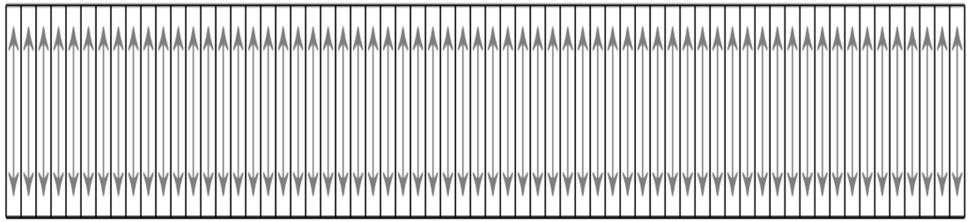
3 operations in a round

1st round computation

On 320-bit state = 5 x 64-bit words



(1) Constant addition



(2) Substitution *(vertical)*

Input of the first round:

- 128-bit key : $K = (k_0, k_1)$
- 128-bit nonce : $N = (n_0, n_1)$
- 64-bit init. vector : IV

3 operations in a round

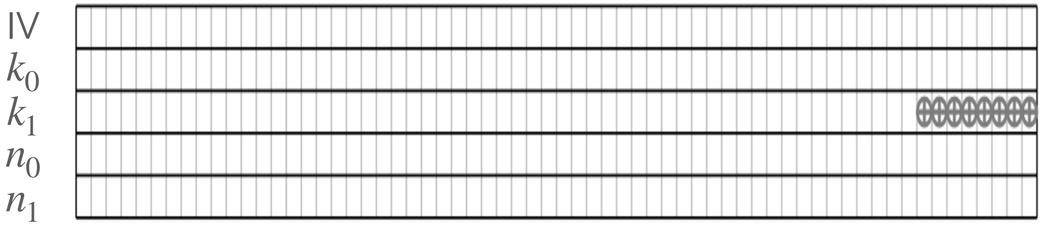
1st round computation

On 320-bit state = 5 x 64-bit words

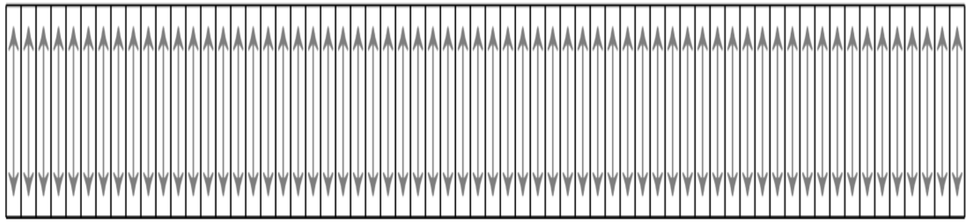
Input of the first round:

- 128-bit key : $K = (k_0, k_1)$
- 128-bit nonce : $N = (n_0, n_1)$
- 64-bit init. vector : IV

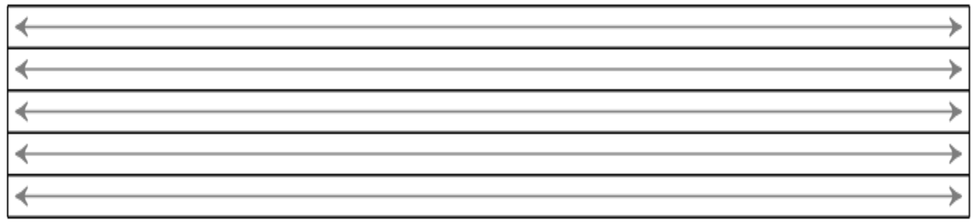
3 operations in a round



(1) Constant addition

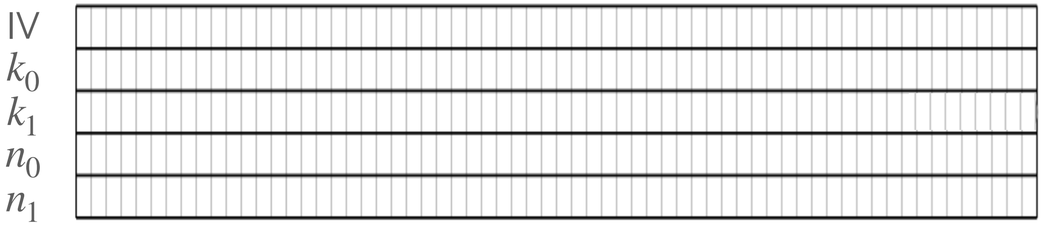


(2) Substitution *(vertical)*

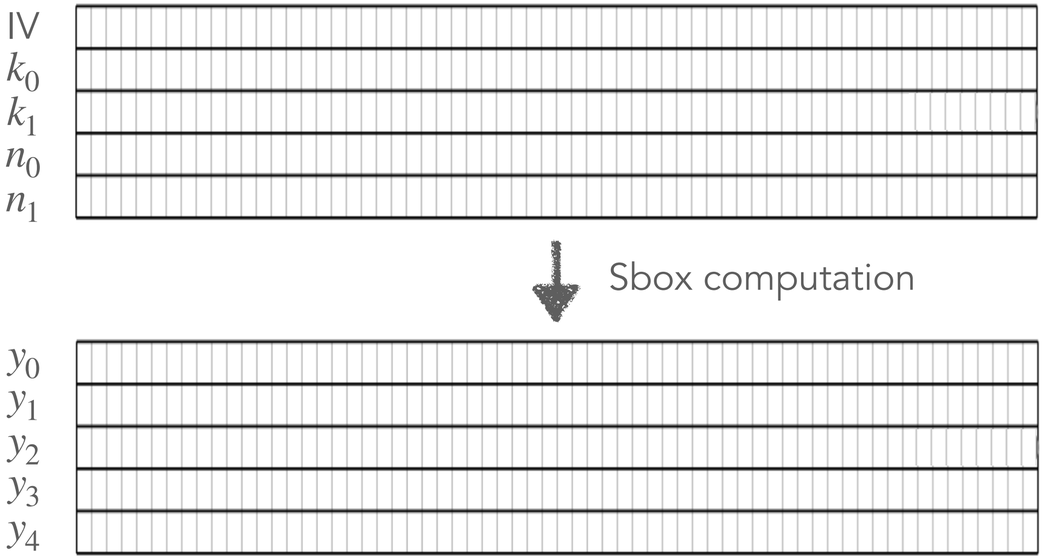


(3) Linear diffusion *(horizontal)*

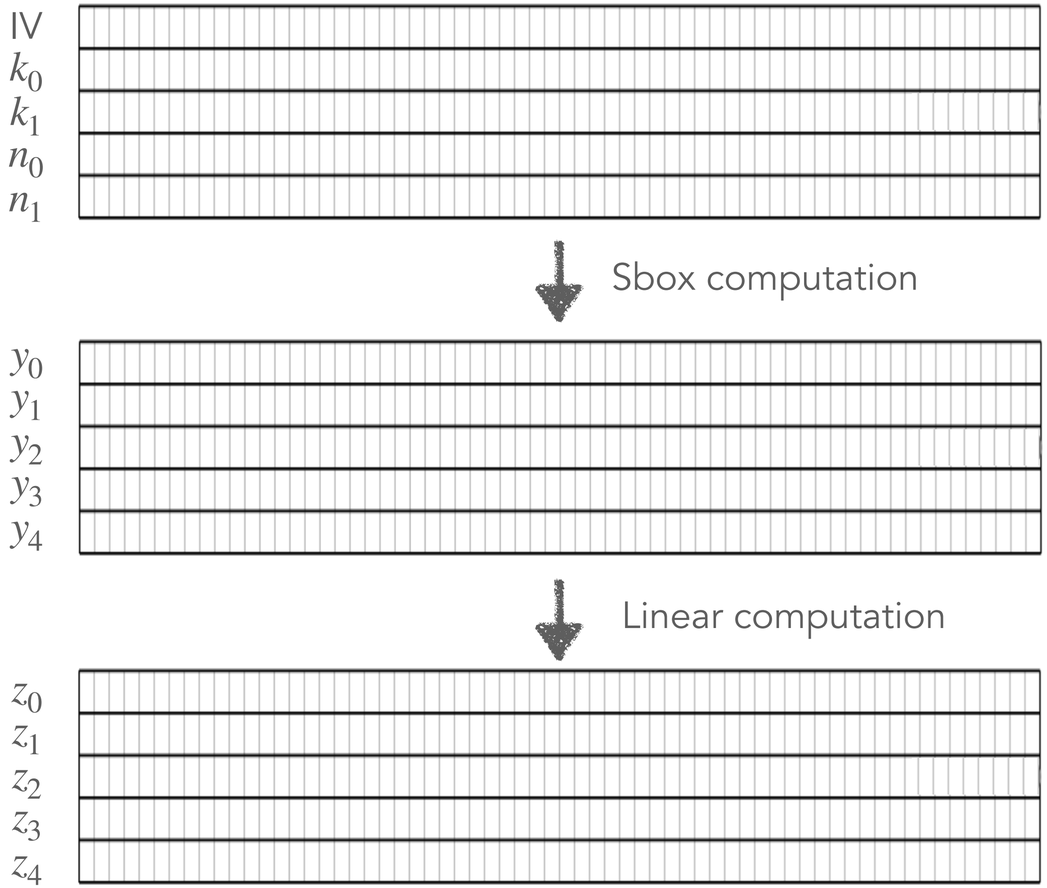
State changes in 1st round



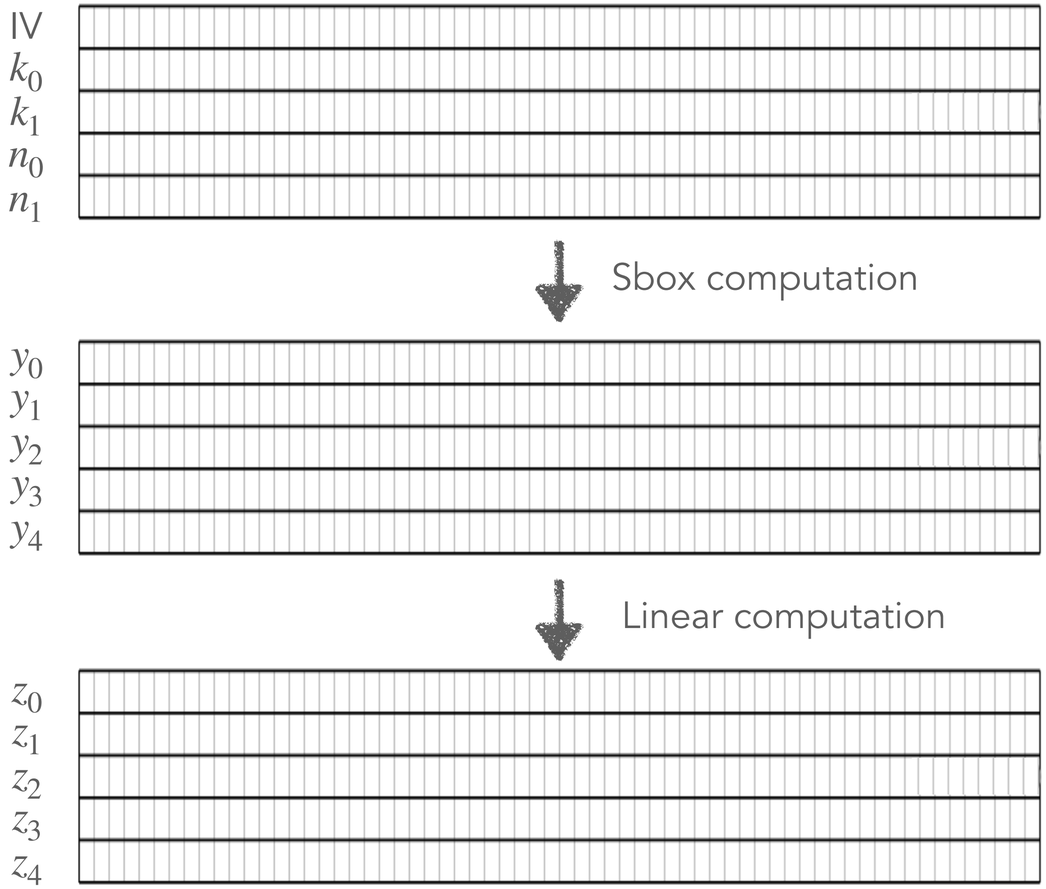
State changes in 1st round



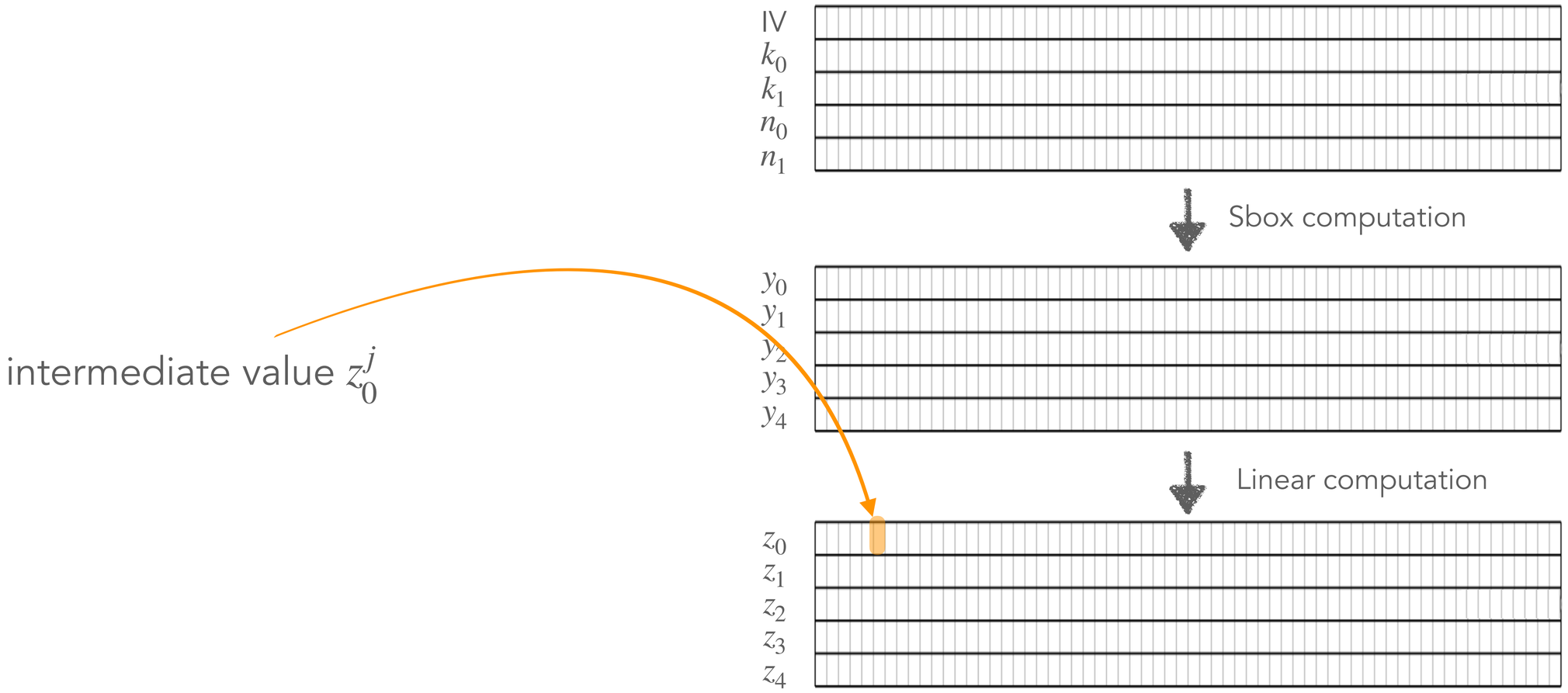
State changes in 1st round



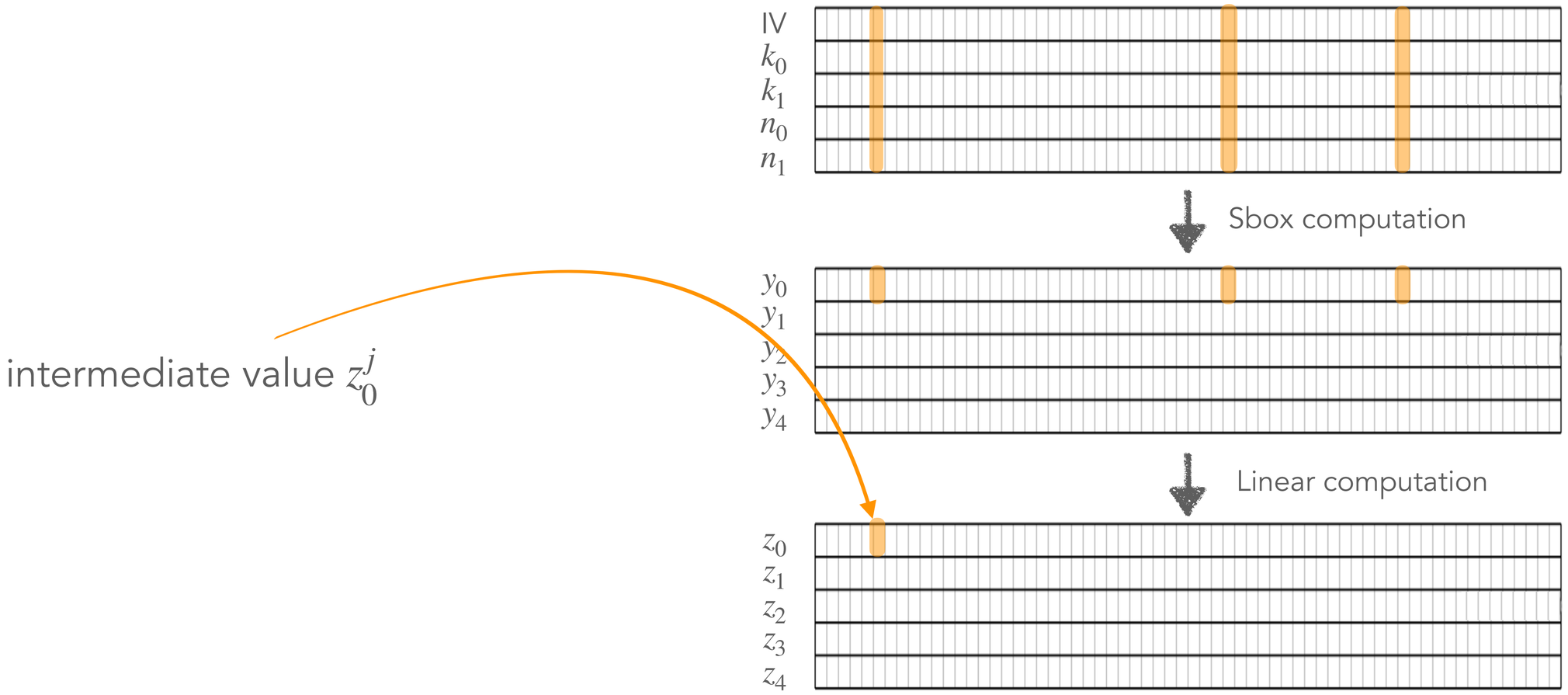
Apply Dobraunig et al.'s attack strategy



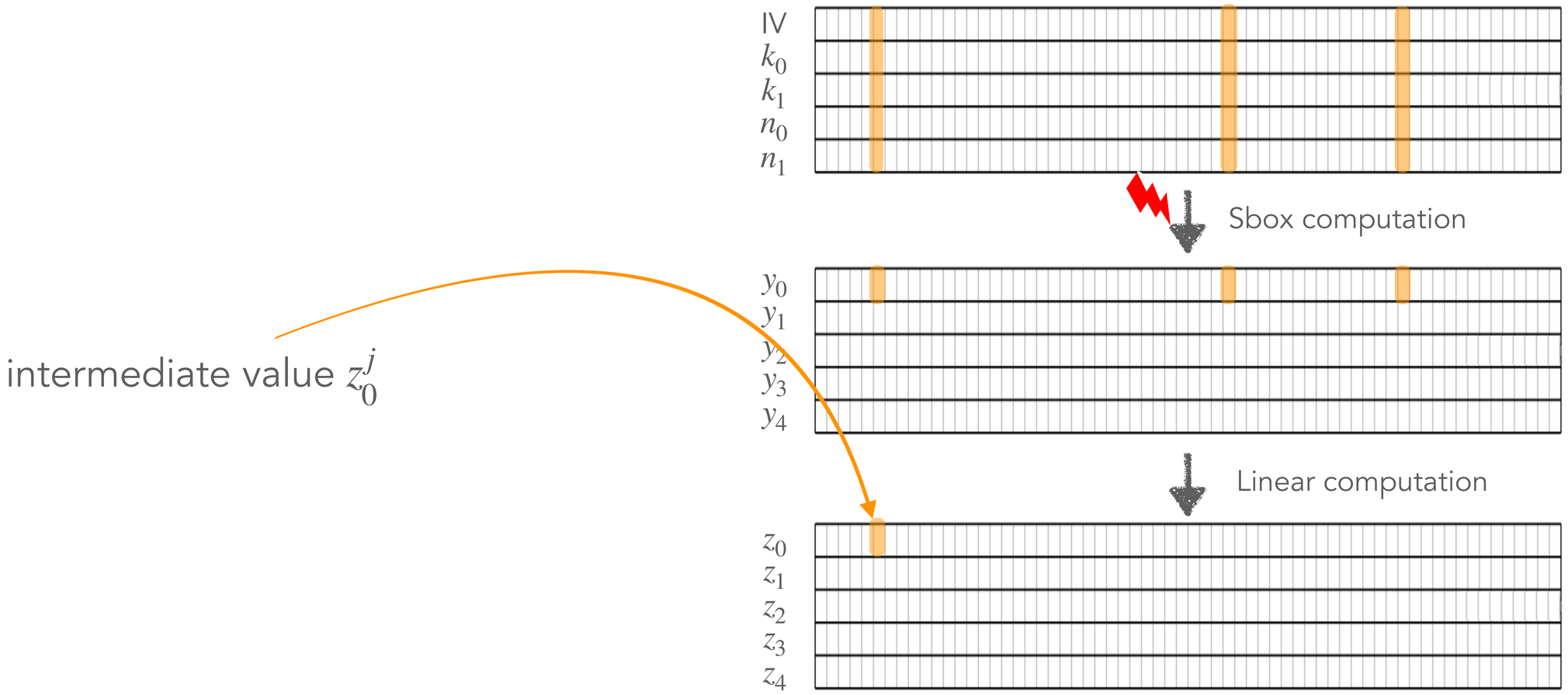
Apply Dobraunig et al.'s attack strategy



Apply Dobraunig et al.'s attack strategy



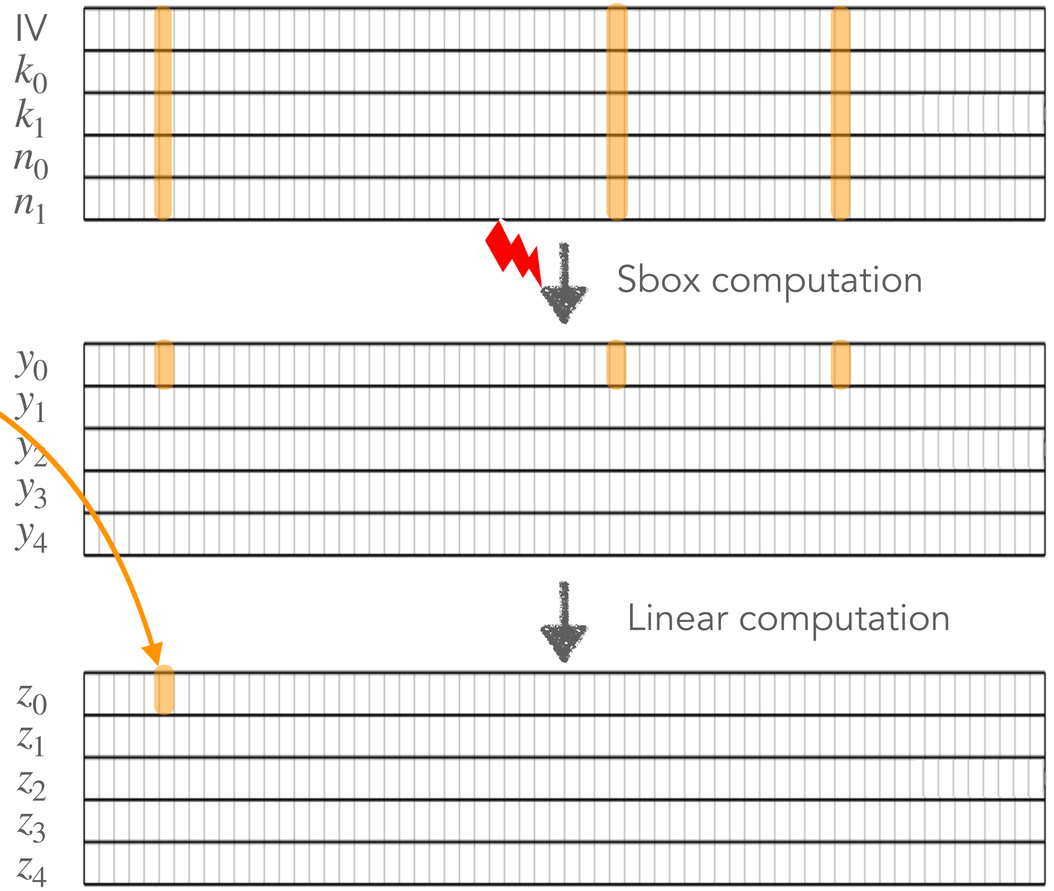
Apply Dobraunig et al.'s attack strategy



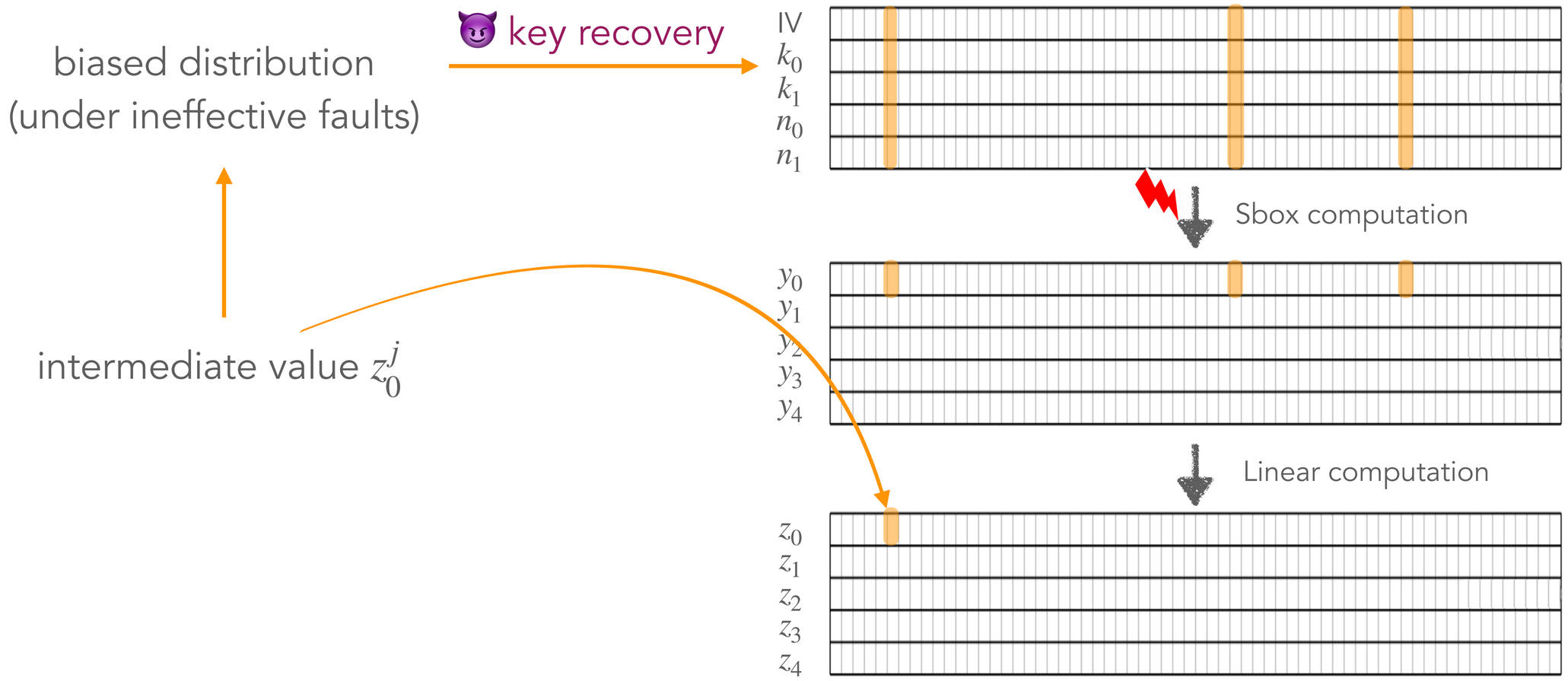
Apply Dobraunig et al.'s attack strategy

biased distribution
(under ineffective faults)

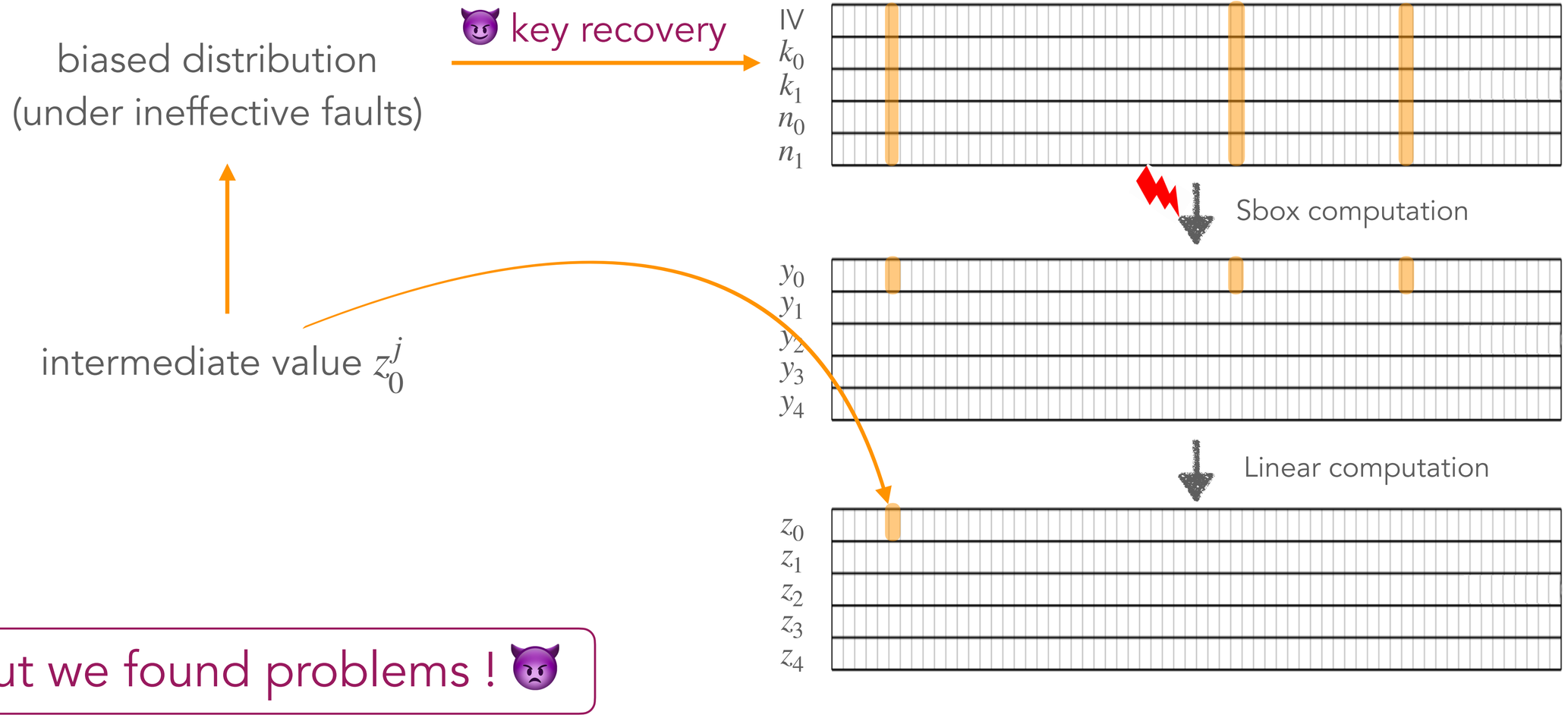
intermediate value z_0^j



Apply Dobraunig et al.'s attack strategy



Apply Dobraunig et al.'s attack strategy



But we found problems ! 😈

Problem 1:
Possibly impractical to have enough ineffective faults

Problem 1:
Possibly impractical to have enough ineffective faults

(with instruction-skip faults)

Instruction skip: XOR

Instruction skip: XOR

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$

$\cdots$

$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$

$\cdots$

$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$

Scenario $1 : \mathrm{R}_2 = \mathrm{R}_1 \oplus \mathrm{R}_0$

Instruction skip: XOR

	No fault	Fault occurs

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$

$\cdots$

$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$

$\cdots$

$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$

$\cdots$

$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$

$\cdots$

$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

No fault	Fault occurs
$R_2 = v_2$	

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	
$\cdots$		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	
$\cdots$		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$		

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	v_2 is used

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	v_2 is used

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Ineffective fault if $v_2 = v_2'$

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	v_2 is used

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform,

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP}_0$ $\mathtt{R}_2$ $-$ $-$	$R_2 = v_2$	$R_2 = v_2$
…		
XOR $\mathtt{R}_2$ $\mathtt{R}_1$ $\mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP}_2$ $-$ $\mathtt{R}_2$ $-$	v_2' is used	v_2 is used

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform, then $\Pr[v_2 = v_2'] = 0.5^w$, w is register bit-width

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$	v_2' is used	v_2 is used

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform, then $\Pr[v_2 = v_2'] = 0.5^w$, w is register bit-width

Architecture	8-bit	32-bit	64-bit
$\Pr[v_2 = v_2']$			

Instruction skip: XOR

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$

$\cdots$

$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$

$\cdots$

$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

	No fault	Fault occurs
	$R_2 = v_2$	$R_2 = v_2$
	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
	v_2' is used	v_2 is used

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform, then $\Pr[v_2 = v_2'] = 0.5^w$, w is register bit-width

Architecture	8-bit	32-bit	64-bit
$\Pr[v_2 = v_2']$	≈ 0.0039		

Instruction skip: XOR

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$

$\cdots$

$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$

$\cdots$

$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

	No fault	Fault occurs
	$R_2 = v_2$	$R_2 = v_2$
	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
	v_2' is used	v_2 is used

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform, then $\Pr[v_2 = v_2'] = 0.5^w$, w is register bit-width

Architecture	8-bit	32-bit	64-bit
$\Pr[v_2 = v_2']$	≈ 0.0039	≈ 0	
	😈	😈	

Instruction skip: XOR

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$

$\cdots$

$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$

$\cdots$

$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

	No fault	Fault occurs
	$R_2 = v_2$	$R_2 = v_2$
	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
	v_2' is used	v_2 is used

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform, then $\Pr[v_2 = v_2'] = 0.5^w$, w is register bit-width

Architecture	8-bit	32-bit	64-bit
$\Pr[v_2 = v_2']$	≈ 0.0039	≈ 0	≈ 0
	😈	😈	😈

Instruction skip: XOR

	No fault	Fault occurs
$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$	$R_2 = v_2$	$R_2 = v_2$
…		
$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$	$R_2 = v_2' = v_1 \oplus v_0$	(skipped)
…		
$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$	v_2' is used	v_2 is used

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

Ineffective fault if $v_2 = v_2'$

Suppose v_0, v_1, v_2 are uniform, then $\Pr[v_2 = v_2'] = 0.5^w$, w is register bit-width

Architecture	8-bit	32-bit	64-bit
$\Pr[v_2 = v_2']$	≈ 0.0039	≈ 0	≈ 0
	😈	😈	😈

Impractical to obtain ineffective fault ! 😈

Instruction skip: XOR

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$
…	
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$
…	
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

$\mathtt{OP}_0$ $\mathtt{R}_2$ $-$ $-$	$R_2 = v_2$	
...		
XOR $\mathtt{R}_2$ $\mathtt{R}_1$ $\mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	→ in ARM
...		
$\mathtt{OP}_2$ $-$ $\mathtt{R}_2$ $-$	v_2' is used	

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

Instruction skip: XOR

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$ $\qquad R_2 = v_2$

$\cdots$

$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$ $\qquad R_2 = v_2' = v_1 \oplus v_0$ $\qquad \rightarrow$ in ARM

$\cdots$

$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$ $\qquad v_2'$ is used

Scenario $1 : \mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$

$\cdots$

$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_2 \quad \mathtt{R}_0$

$\cdots$

$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$

Scenario $2 : \mathtt{R}_2 = \mathtt{R}_2 \oplus \mathtt{R}_0$

Instruction skip: XOR

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$	
…		
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	→ in ARM
…		
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used	

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$
…	
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_2 \quad \mathtt{R}_0$	
…	
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	

Scenario 2 : $\mathtt{R}_2 = \mathtt{R}_2 \oplus \mathtt{R}_0$

Instruction skip: XOR

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$	$R_2 = v_2$	
…		
$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$	$R_2 = v_2' = v_1 \oplus v_0$	→ in ARM
…		
$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$	v_2' is used	

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$	$R_2 = v_2$
…	
$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_2}\ \ \mathtt{R_0}$	$R_2 = v_2' = v_2 \oplus v_0$
…	
$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$	

Scenario 2 : $\mathtt{R_2} = \mathtt{R_2} \oplus \mathtt{R_0}$

Instruction skip: XOR

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$	$R_2 = v_2$
…	
$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_1}\ \ \mathtt{R_0}$	$R_2 = v_2' = v_1 \oplus v_0$ → in ARM
…	
$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$	v_2' is used

Scenario 1 : $\mathtt{R_2} = \mathtt{R_1} \oplus \mathtt{R_0}$

$\mathtt{OP_0}\ \ \mathtt{R_2}\ \ -\ \ -$	$R_2 = v_2$
…	
$\mathtt{XOR}\ \ \mathtt{R_2}\ \ \mathtt{R_2}\ \ \mathtt{R_0}$	$R_2 = v_2' = v_2 \oplus v_0$
…	
$\mathtt{OP_2}\ \ -\ \ \mathtt{R_2}\ \ -$	

Scenario 2 : $\mathtt{R_2} = \mathtt{R_2} \oplus \mathtt{R_0}$

Instruction skip: XOR

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$
…	
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_1 \quad \mathtt{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$
…	
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used

Scenario 1 : $\mathtt{R}_2 = \mathtt{R}_1 \oplus \mathtt{R}_0$

→ in ARM

$\mathtt{OP}_0 \quad \mathtt{R}_2 \quad - \quad -$	$R_2 = v_2$
…	
$\mathtt{XOR} \quad \mathtt{R}_2 \quad \mathtt{R}_2 \quad \mathtt{R}_0$	$R_2 = v_2' = v_2 \oplus v_0$
…	
$\mathtt{OP}_2 \quad - \quad \mathtt{R}_2 \quad -$	v_2' is used

Scenario 2 : $\mathtt{R}_2 = \mathtt{R}_2 \oplus \mathtt{R}_0$

Instruction skip: XOR

$\mathrm{OP}_0 \quad \mathrm{R}_2 \quad - \quad -$	$R_2 = v_2$	
…		
XOR $\mathrm{R}_2 \quad \mathrm{R}_1 \quad \mathrm{R}_0$	$R_2 = v_2' = v_1 \oplus v_0$	→ in ARM
…		
$\mathrm{OP}_2 \quad - \quad \mathrm{R}_2 \quad -$	v_2' is used	

Scenario 1 : $\mathrm{R}_2 = \mathrm{R}_1 \oplus \mathrm{R}_0$

$\mathrm{OP}_0 \quad \mathrm{R}_2 \quad - \quad -$	$R_2 = v_2$	
…		
XOR $\mathrm{R}_2 \quad \mathrm{R}_2 \quad \mathrm{R}_0$	$R_2 = v_2' = v_2 \oplus v_0$	→ in AVR
…		
$\mathrm{OP}_2 \quad - \quad \mathrm{R}_2 \quad -$	v_2' is used	

Scenario 2 : $\mathrm{R}_2 = \mathrm{R}_2 \oplus \mathrm{R}_0$

Instruction skip: XOR, AND, NOT

XOR (scenario 1) $\Pr[v_2 = v_2'] = 0.5^w$

XOR (scenario 2) $\Pr[v_2 = v_2'] = 0.5^w$

Instruction skip: XOR, AND, NOT

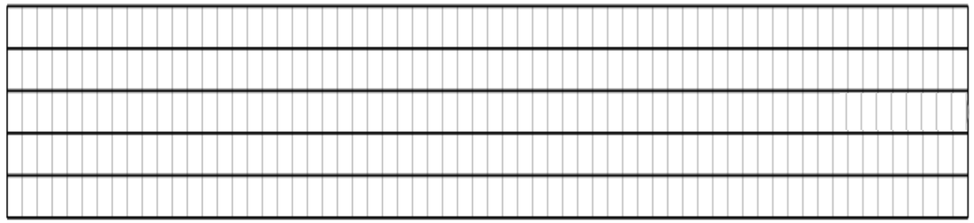
XOR (scenario 1)	$\Pr[v_2 = v_2'] = 0.5^w$
XOR (scenario 2)	$\Pr[v_2 = v_2'] = 0.5^w$
AND (scenario 1)	$\Pr[v_2 = v_2'] = 0.5^w$
AND (scenario 2)	$\Pr[v_2 = v_2'] = 0.75^w$

Instruction skip: XOR, AND, NOT

XOR (scenario 1)	$\Pr[v_2 = v_2'] = 0.5^w$
XOR (scenario 2)	$\Pr[v_2 = v_2'] = 0.5^w$
AND (scenario 1)	$\Pr[v_2 = v_2'] = 0.5^w$
AND (scenario 2)	$\Pr[v_2 = v_2'] = 0.75^w$
NOT (scenario 1)	$\Pr[v_2 = v_2'] = 0.5^w$
NOT (scenario 2)	0

Implementations of Ascon

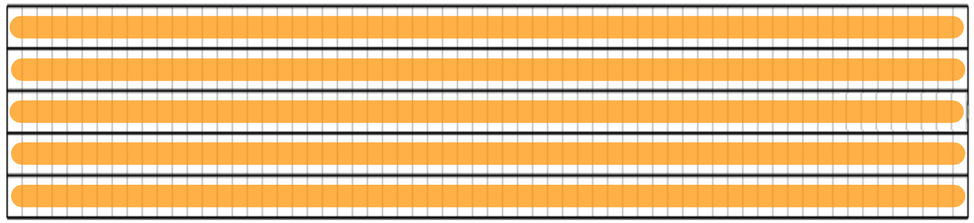
On 320-bit state = 5 x 64-bit words



Implementations of Ascon

On 320-bit state = 5 x 64-bit words

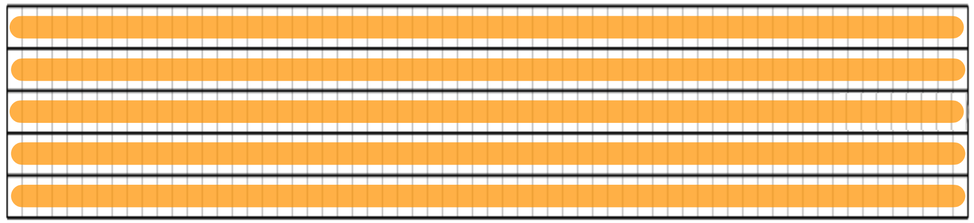
64-bit implementation →



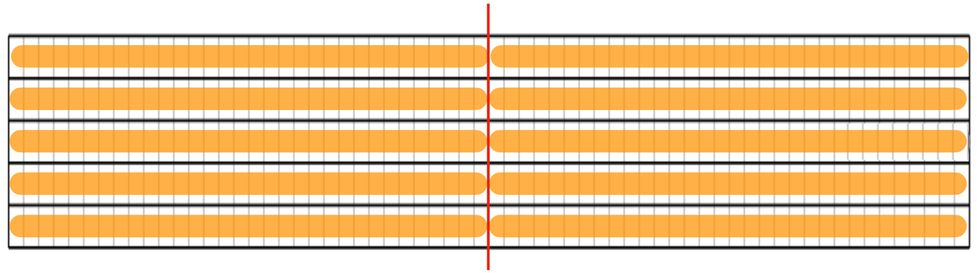
Implementations of Ascon

On 320-bit state = 5 x 64-bit words

64-bit implementation →



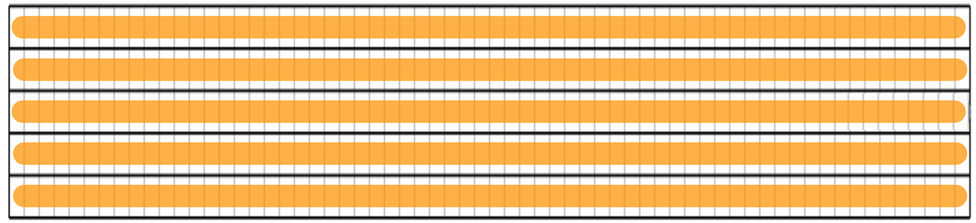
32-bit implementation →



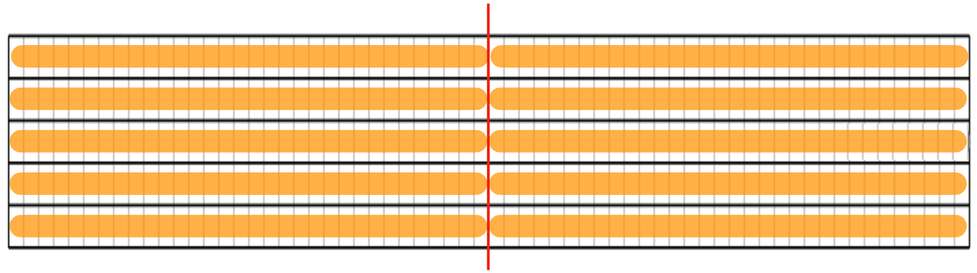
Implementations of Ascon

On 320-bit state = 5 x 64-bit words

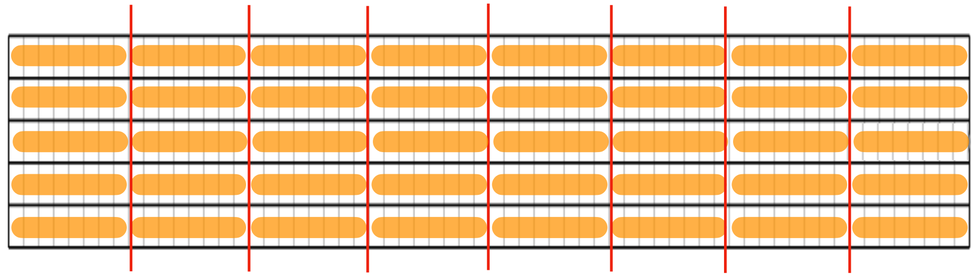
64-bit implementation →



32-bit implementation →



8-bit implementation →



Apply to 8-bit implementation of Ascon

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1			
XOR S2			
AND S1			
AND S2			
NOT S1			
NOT S2			

Apply to 8-bit implementation of Ascon

- $w = 8$

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1			
XOR S2			
AND S1			
AND S2			
NOT S1			
NOT S2			

Apply to 8-bit implementation of Ascon

- $w = 8$

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1			0.0039
XOR S2			0.0039
AND S1			0.0039
AND S2			0.1001
NOT S1			0.0039
NOT S2			0

Apply to 8-bit implementation of Ascon

- $w = 8$
- 20,000 executions with random inputs

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1			0.0039
XOR S2			0.0039
AND S1			0.0039
AND S2			0.1001
NOT S1			0.0039
NOT S2			0

Apply to 8-bit implementation of Ascon

- $w = 8$
- 20,000 executions with random inputs

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1	81		0.0039
XOR S2	79		0.0039
AND S1	80		0.0039
AND S2	2011		0.1001
NOT S1	74		0.0039
NOT S2	0		0

Apply to 8-bit implementation of Ascon

- $w = 8$
- 20,000 executions with random inputs

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1	81	0.0040	0.0039
XOR S2	79	0.0040	0.0039
AND S1	80	0.0040	0.0039
AND S2	2011	0.1006	0.1001
NOT S1	74	0.0037	0.0039
NOT S2	0	0	0

Apply to 8-bit implementation of Ascon

- $w = 8$
- 20,000 executions with random inputs

Skipped Instruction	# Ineffective Faults	Empirical Probability	Theoretical Probability
XOR S1	81	0.0040	0.0039
XOR S2	79	0.0040	0.0039
AND S1	80	0.0040	0.0039
AND S2	2011	0.1006	0.1001
NOT S1	74	0.0037	0.0039
NOT S2	0	0	0

This confirms our analysis ✅

Problem 2:
Intermediate value remains uniform

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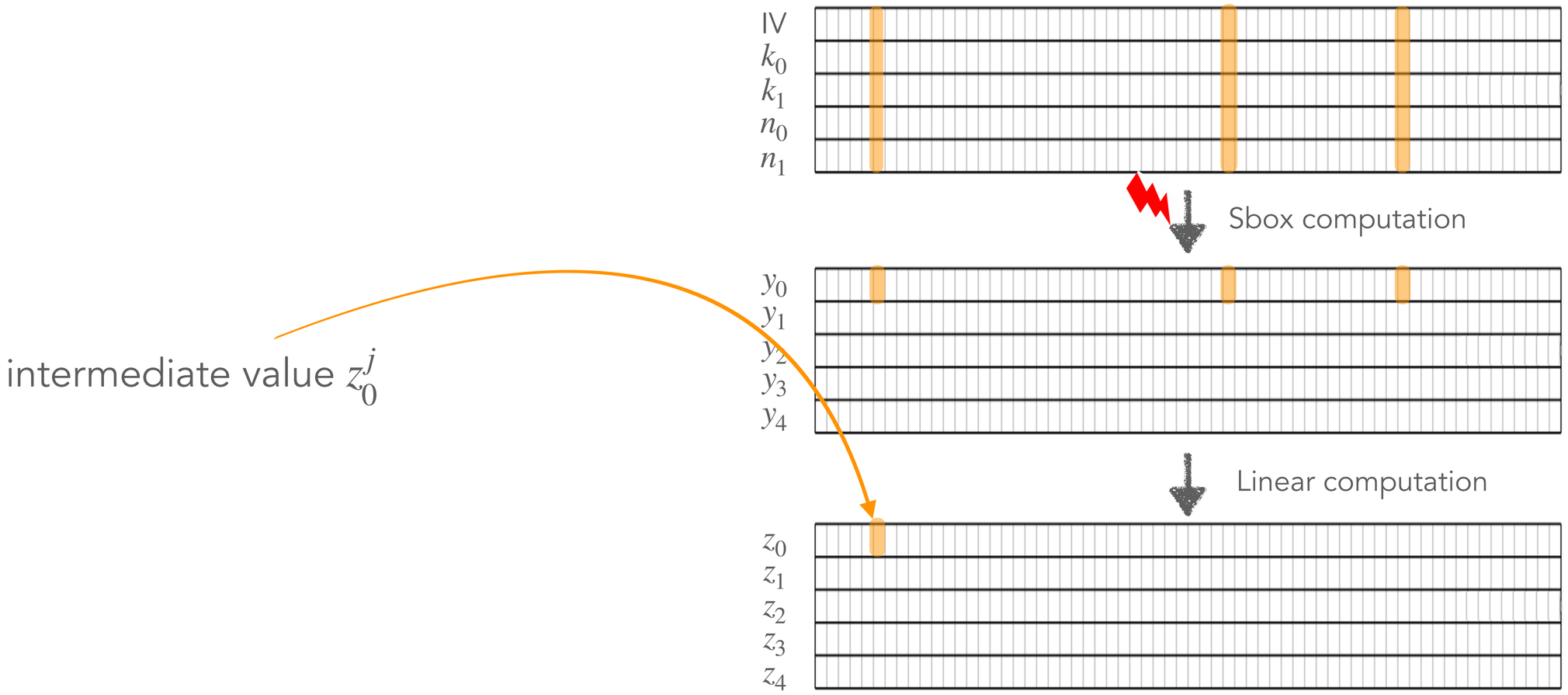
Intermediate value remains uniform

(with instruction-skip on 8-bit implementation)

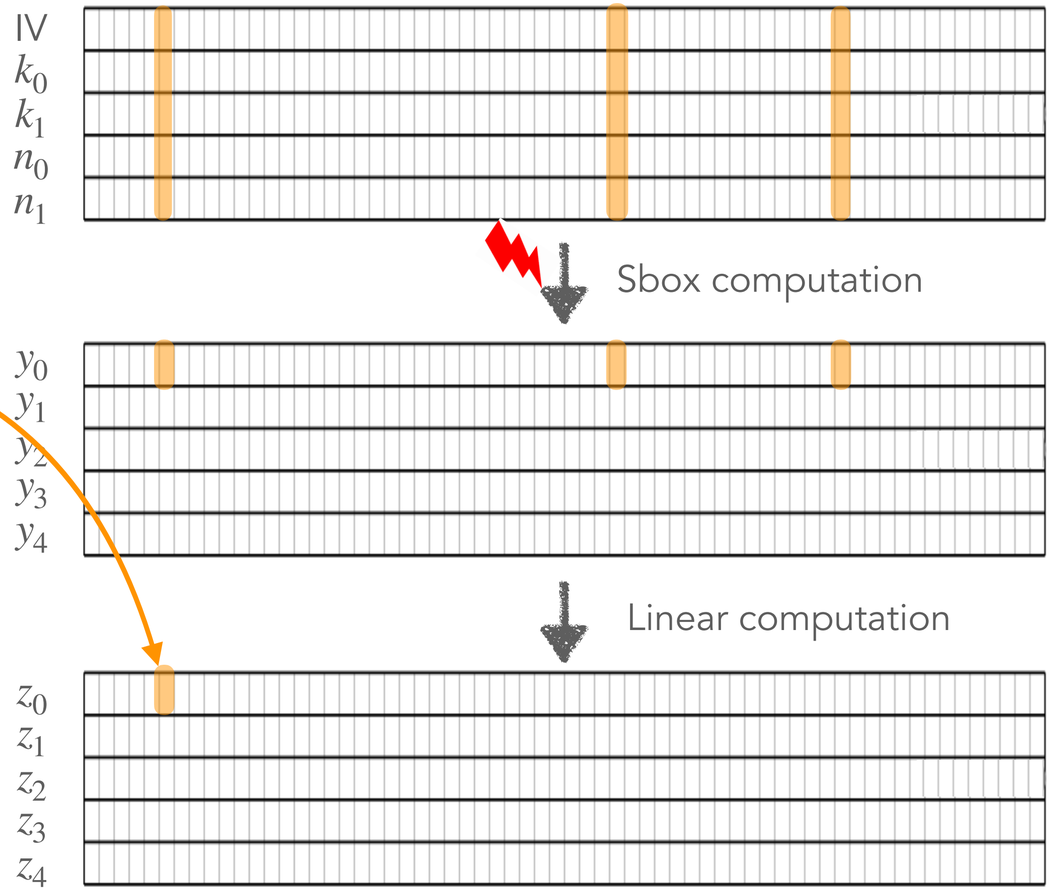
Apply Dobraunig et al.'s attack strategy



Apply Dobraunig et al.'s attack strategy

intermediate value z_0^j

$$z_0^j = y_0^j \oplus y_0^{j+19} \oplus y_0^{j+45}$$



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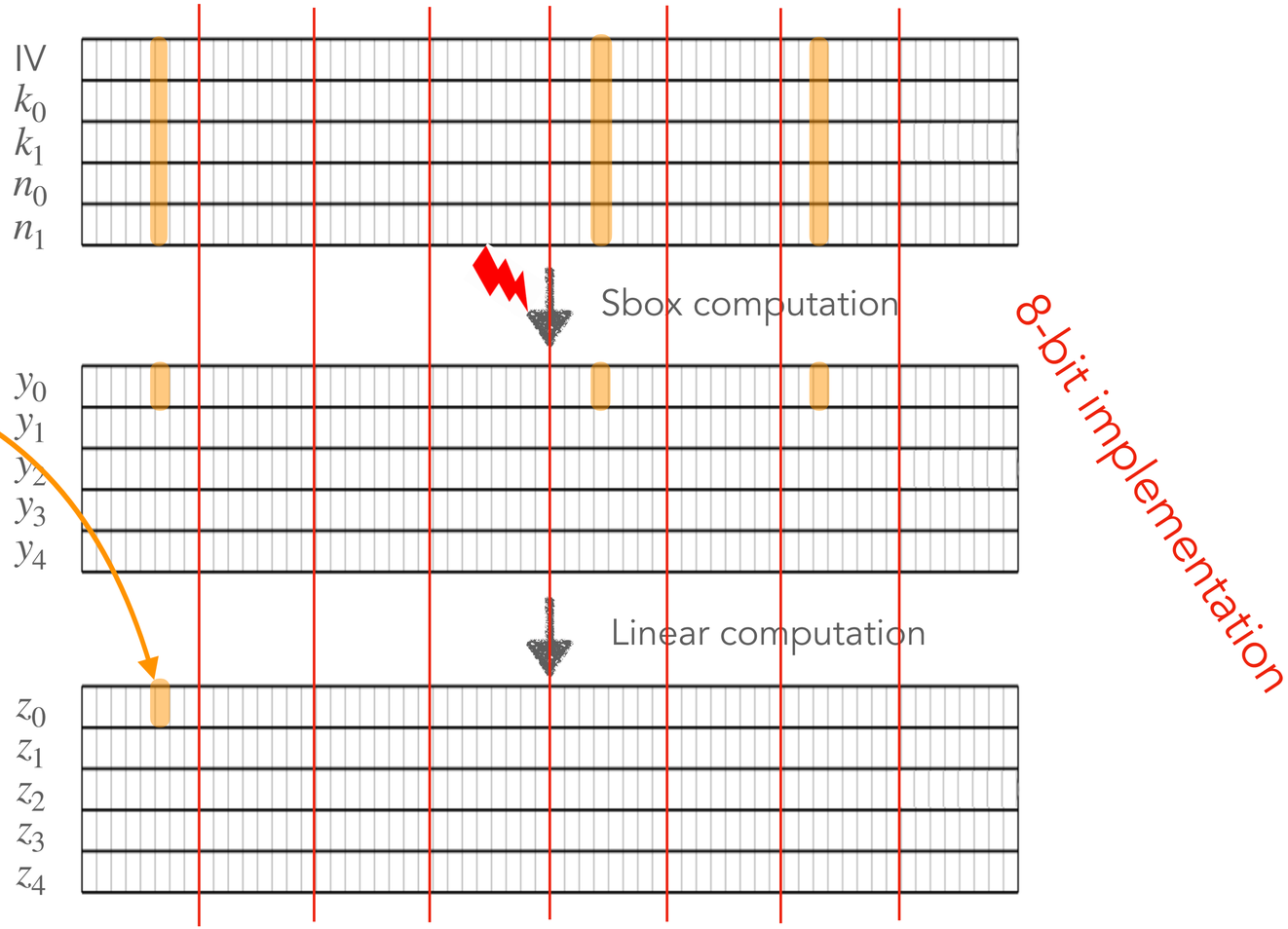

Apply Dobraunig et al.'s attack strategy

An instruction skip does not affect <u>all</u> 3 bits

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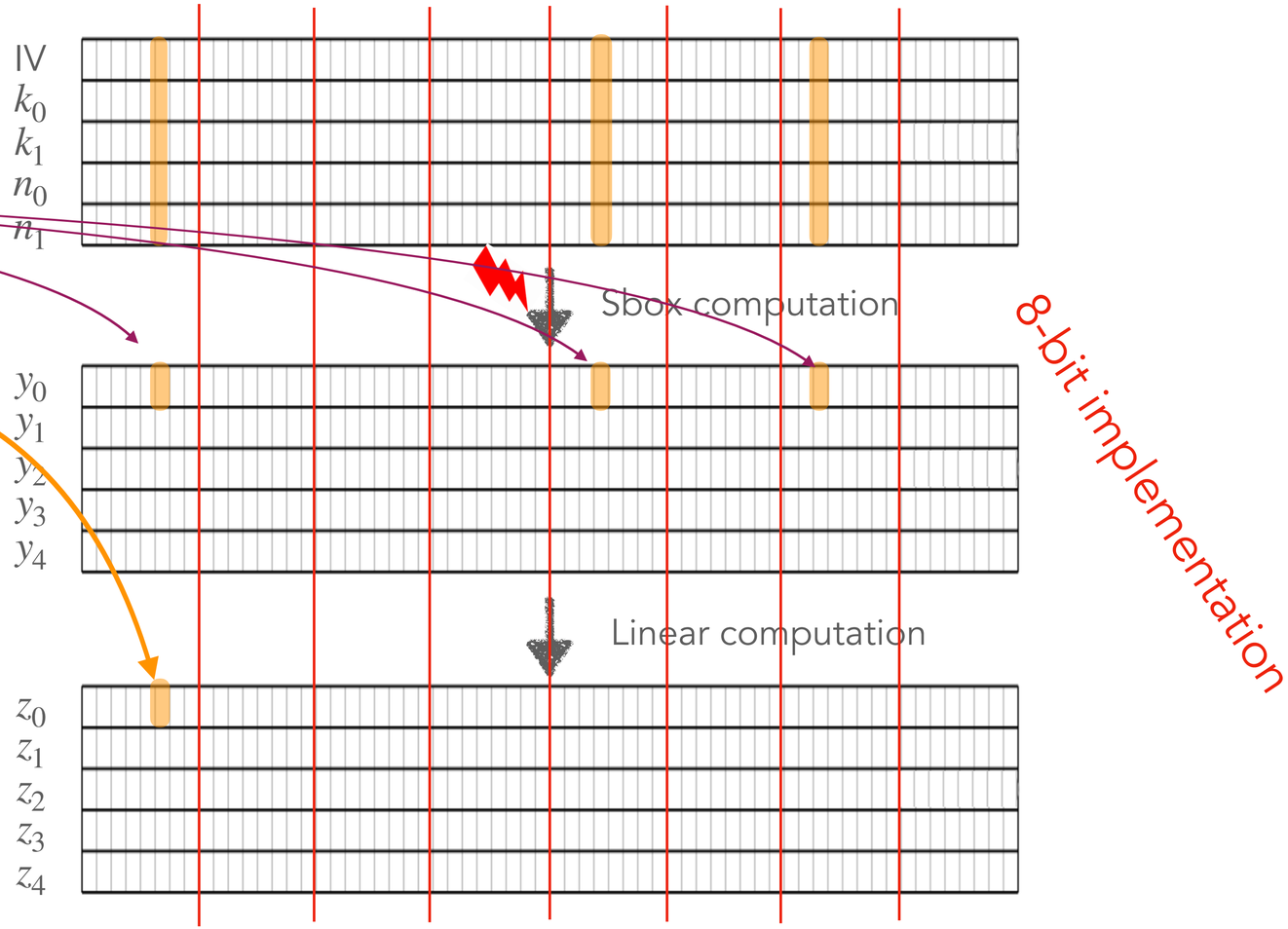

Apply Dobraunig et al.'s attack strategy

An instruction skip
does not affect <u>all</u> 3 bits

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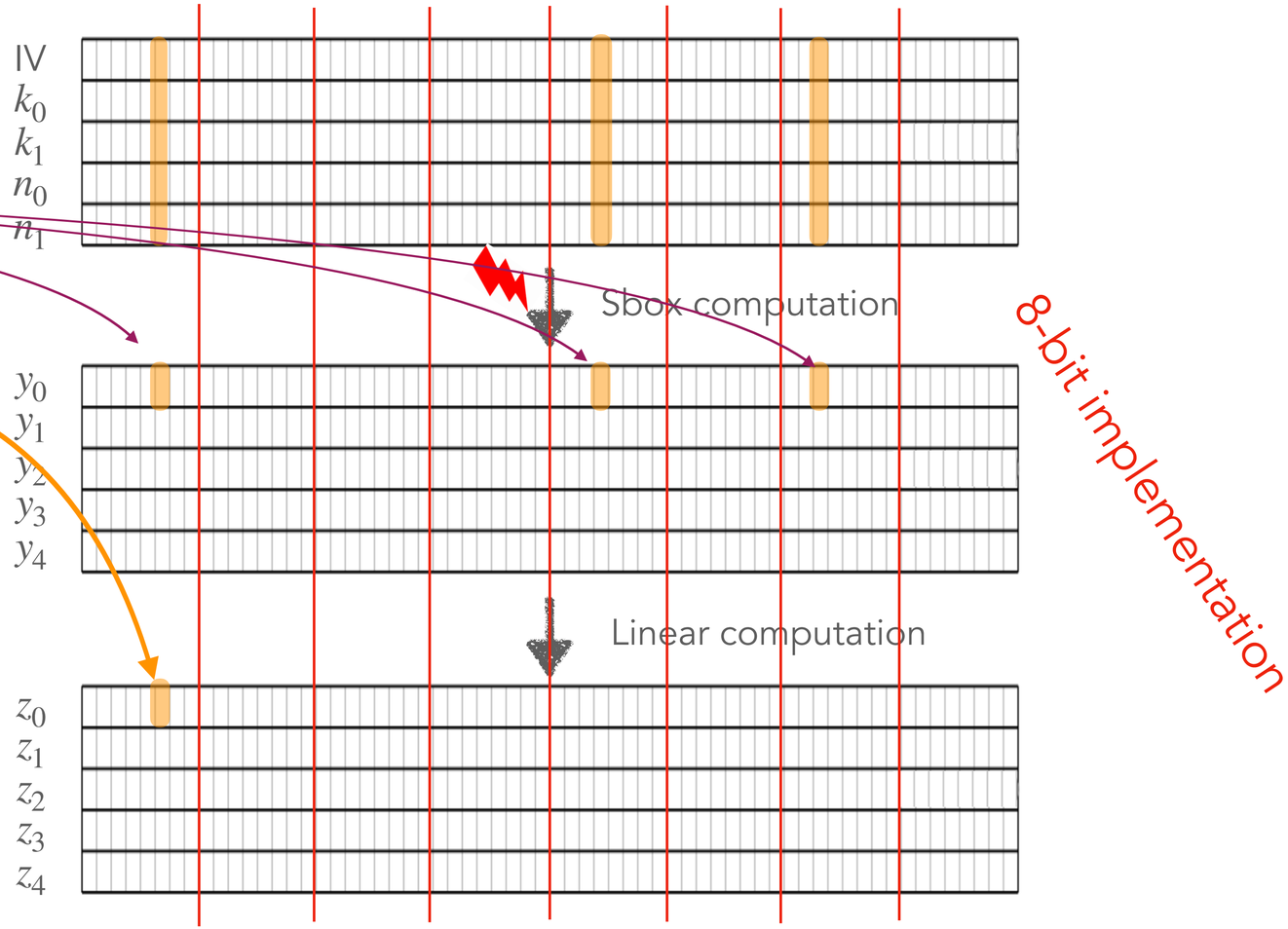
→ z_0^j remains uniform



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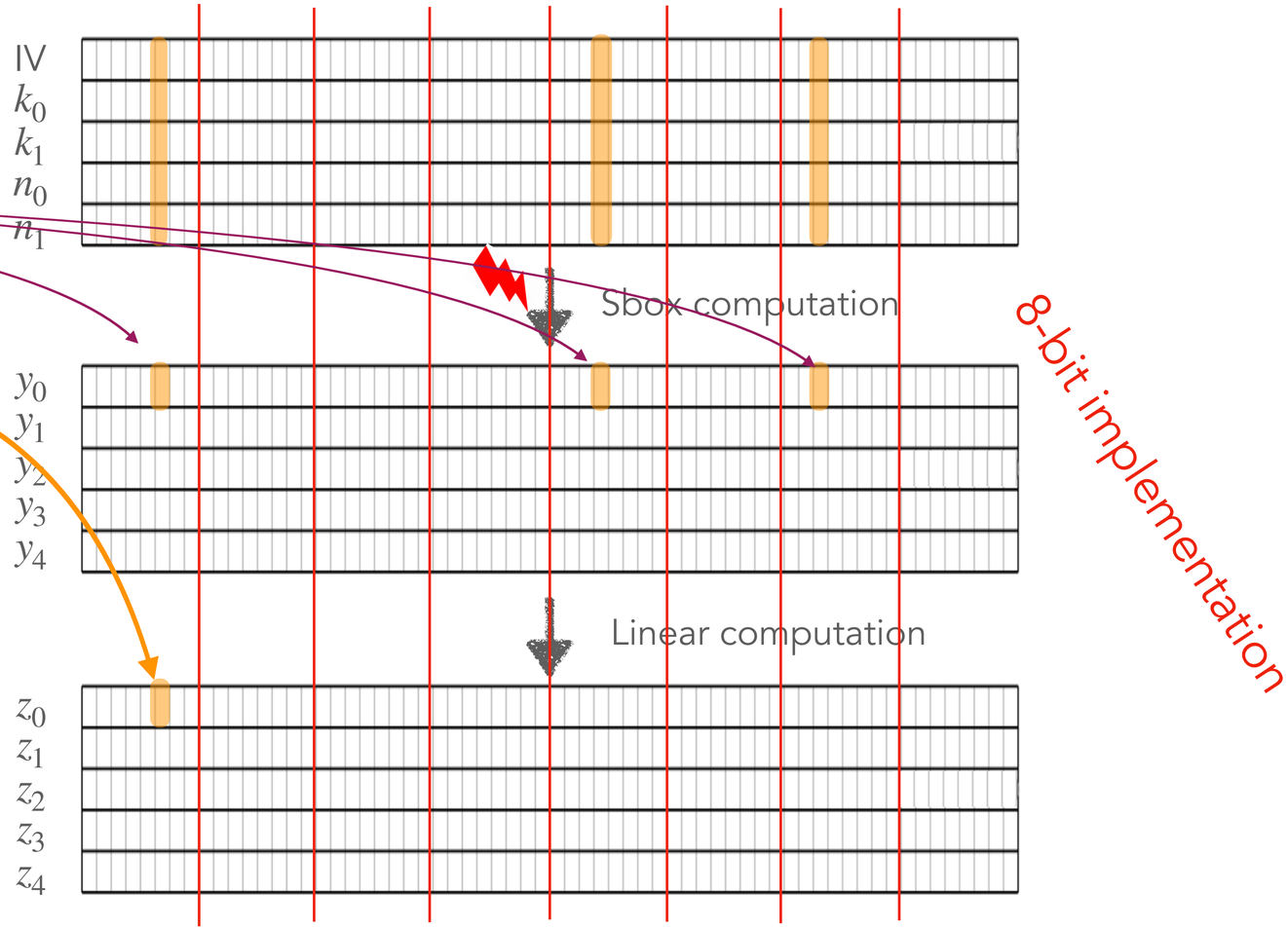
An instruction skip does not affect <u>all</u> 3 bits

intermediate value z_0^j

$$z_0^j = y_0^j \oplus y_0^{j+19} \oplus y_0^{j+45}$$

→ z_0^j remains uniform

→ SIFA is not applicable 😈



Apply Dobraunig et al.'s attack strategy

An instruction skip
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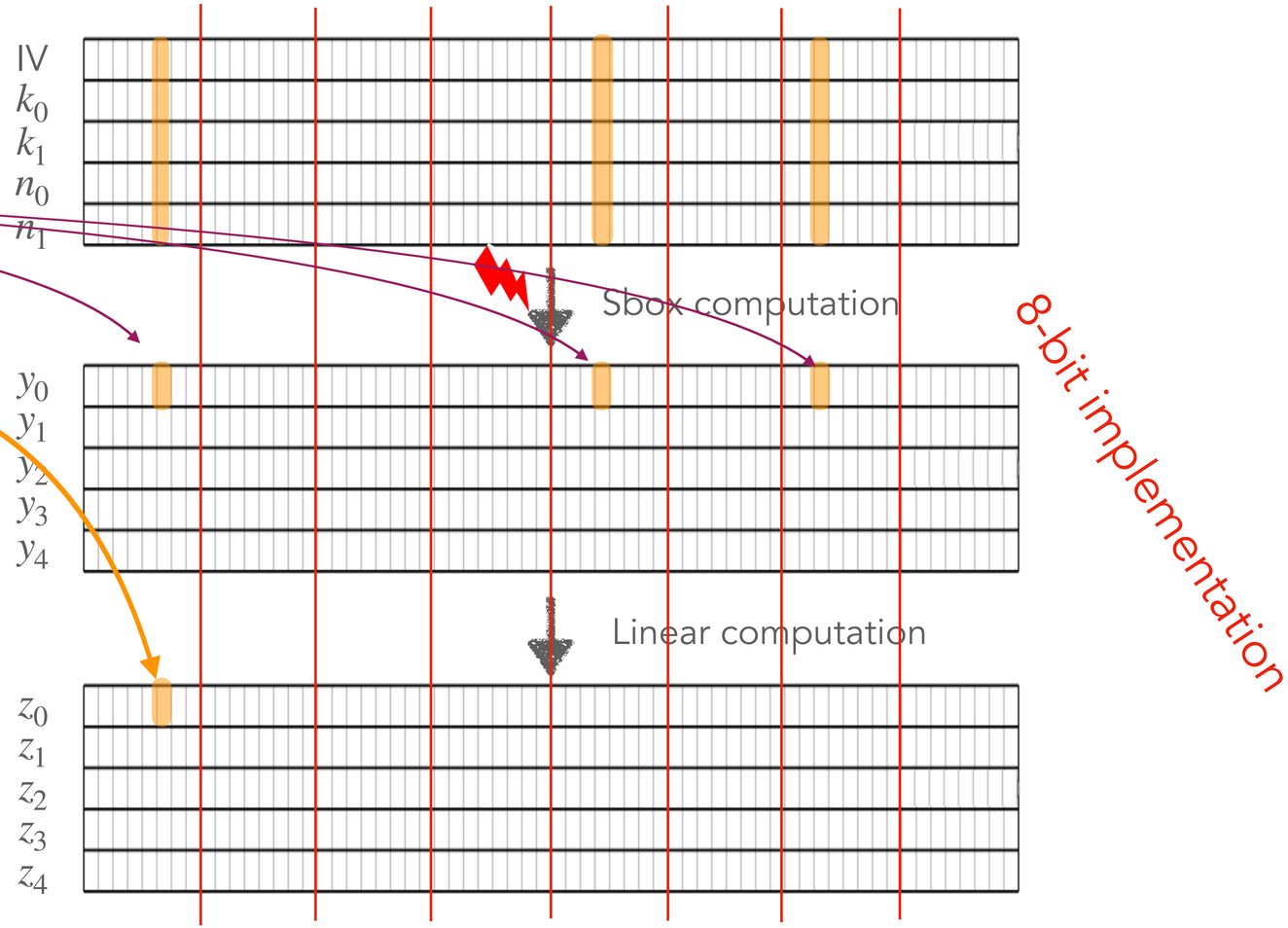
intermediate value z_0^j

$$z_0^j = y_0^j \oplus y_0^{j+19} \oplus y_0^{j+45}$$

→ z_0^j remains uniform

→ SIFA is not applicable 😈

Need formal proof? 🤔 → read our paper 📄



Apply to 8-bit implementation of Ascon

Skipped Instruction	# Ineff. Faults	Emp. Prob. (Pr[0] / Pr[1])	Theo. Prob. (Pr[0] / Pr[1])
XOR S1			
XOR S2			
AND S1			
AND S2			
NOT S1			
NOT S2			

Apply to 8-bit implementation of Ascon

- $w = 8$

Skipped Instruction	# Ineff. Faults	Emp. Prob. (Pr[0] / Pr[1])	Theo. Prob. (Pr[0] / Pr[1])
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Apply to 8-bit implementation of Ascon

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Skipped Instruction	# Ineff. Faults	Emp. Prob. (Pr[0] / Pr[1])	Theo. Prob. (Pr[0] / Pr[1])
XOR S1			0.5 / 0.5
XOR S2			0.5 / 0.5
AND S1			0.5 / 0.5
AND S2			0.5 / 0.5
NOT S1			0.5 / 0.5
NOT S2			- / -

Apply to 8-bit implementation of Ascon

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Skipped Instruction	# Ineff. Faults	Emp. Prob. (Pr[0] / Pr[1])	Theo. Prob. (Pr[0] / Pr[1])
XOR S1	81		0.5 / 0.5
XOR S2	79		0.5 / 0.5
AND S1	80		0.5 / 0.5
AND S2	2011		0.5 / 0.5
NOT S1	74		0.5 / 0.5
NOT S2	0		- / -

Apply to 8-bit implementation of Ascon

- $w = 8$
- 20,000 executions with random inputs

Skipped Instruction	# Ineff. Faults	Emp. Prob. (Pr[0] / Pr[1])	Theo. Prob. (Pr[0] / Pr[1])
XOR S1	81	0.54 / 0.46	0.5 / 0.5
XOR S2	79	0.44 / 0.56	0.5 / 0.5
AND S1	80	0.53 / 0.47	0.5 / 0.5
AND S2	2011	0.52 / 0.48	0.5 / 0.5
NOT S1	74	0.42 / 0.58	0.5 / 0.5
NOT S2	0	- / -	- / -

Summary

Main points

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- Probability of an ineffective fault depends on
  - Instruction type
  - Architecture

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Other instructions (OR, ROL,…)? 🤔

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  - demonstrated on 8-bit implementation of Ascon
  - failed to apply SIFA

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- Probability of an ineffective fault depends on
  - Instruction type
  - Architecture

Other instructions (OR, ROL,…)? 🤔

Input data is not uniform? 🤔

- Intermediate value may not unexpectedly be biased
  - demonstrated on 8-bit implementation of Ascon
  - failed to apply SIFA

Choose another intermediate value? 🤔

SIFA on Nonce-based Authenticated Encryption: When does it fail? Application to Ascon

Viet-Sang Nguyen

joint work with Vincent Grosso and Pierre-Louis Cayrel

SESAM Seminars
Saint-Étienne, 3 July 2025

UNIVERSITÉ DE LYON
UNIVERSITÉ JEAN MONNET SAINT-ÉTIENNE
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